National Semiconductor

September 26, 2008

LM49450 Boomer® Audio Power Amplifier Series
I²S Input, 2.5W/Channel, Low EMI, Stereo, Class D Audio Sub-System with Ground Referenced Headphone Amplifier, 3D Enhancement, and Headphone Sense

General Description

The LM49450 is a fully integrated audio subsystem designed for portable media player applications. The LM49450 combines a 24-bit I²S digital-to-analog converter (DAC), 2.5W/channel stereo Class D speaker drivers, 36mW stereo ground referenced headphone drivers, volume control, and National's unique 3D sound enhancement into a single device.

The filterless Class D amplifiers deliver 1.25W/channel into an 8Ω load with <1% THD+N with a 5V supply. The LM49450 offers two logic selectable modulation schemes, fixed frequency mode, and an EMI reducing spread spectrum mode. The 36mW/channel headphone drivers feature National's ground referenced architecture that creates a ground-referenced output from a single supply, eliminating the need for bulky and expensive DC-blocking capacitors, saving space and minimizing system cost. A headphone sense input (HPS) automatically detects the presence of a headphone, and configures the device accordingly.

The LM49450 stereo, 24-bit DAC supports a wide range of sample rates (including 192kHz, 96kHz, 48kHz, and 44.1kHz). The digital audio signal path features better than 100dB SNR, and low 0.05% THD+N when measured at the headphone outputs. The flexible 3-wire I²S interface supports left or right justified audio data.

The LM49450 features separate 32-step volume control for the headphones and speaker outputs. 3D enhancement, mode selection, shutdown control, and volume are controlled through an I²C compatible interface.

Output short circuit and thermal overload protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM49450 is available in a space saving 32-pin LLP package.

Key Specifications

■ SNR at Headphone Output	102dBA (typ)
■ Speaker Amplifier Efficiency at 3.6V, 650mW/channel into 8Ω	87% (typ)
■ Speaker Amplifier Efficiency at 5V, 1.1W/channel into 8Ω	80% (typ)
■ Quiescent Power Supply Current Line Inputs:	
Speaker Mode at LSV_{DD} = 3.6V	7.5mA (typ)
Headphone Mode at HPV_{DD} = 2.5V	5.3mA (typ)
■ Output Power/Channel	
Speaker at LSV_{DD} = 5V:	
R_L = 4Ω, THD+N ≤ 10%	2.5W (typ)
R_L = 8Ω, THD+N ≤ 1%	1.25W (typ)
Headphone at HPV_{DD} = 2.5V:	
R_L = 16Ω, THD+N ≤ 1%	34mW (typ)
R_L = 32Ω, THD+N ≤ 1%	36mW (typ)
■ PSRR at 1kHz	
Speaker Mode	67dB (typ)
Headphone Mode	77dB (typ)
■ Shutdown current	0.02µA (typ)

Features

- 24–Bit Stereo DAC
- Stereo Filterless Class D Operation
- Selectable spread spectrum mode reduces EMI
- Ground Referenced Headphone Amplifiers with 100dB SNR
- I²S Compatible Audio Interface
- Audio Sample Rates up to 192kHz
- National's 3D Enhancement
- 32-step Digital Volume Control
- I²C Compatible Control Interface
- Headphone Sense Input
- Stereo Analog Line Inputs
- Output Short Circuit Protection
- Thermal Overload Protection
- Minimum external components
- Click and Pop suppression
- Micro-power shutdown
- Available in space-saving 32 pin LLP package

Applications

- Portable Media Players
- Portable Navigation Devices
- Multi-Media Monitors
- Laptops
- Portable Gaming Devices
- Mobile Handsets

Typical Application

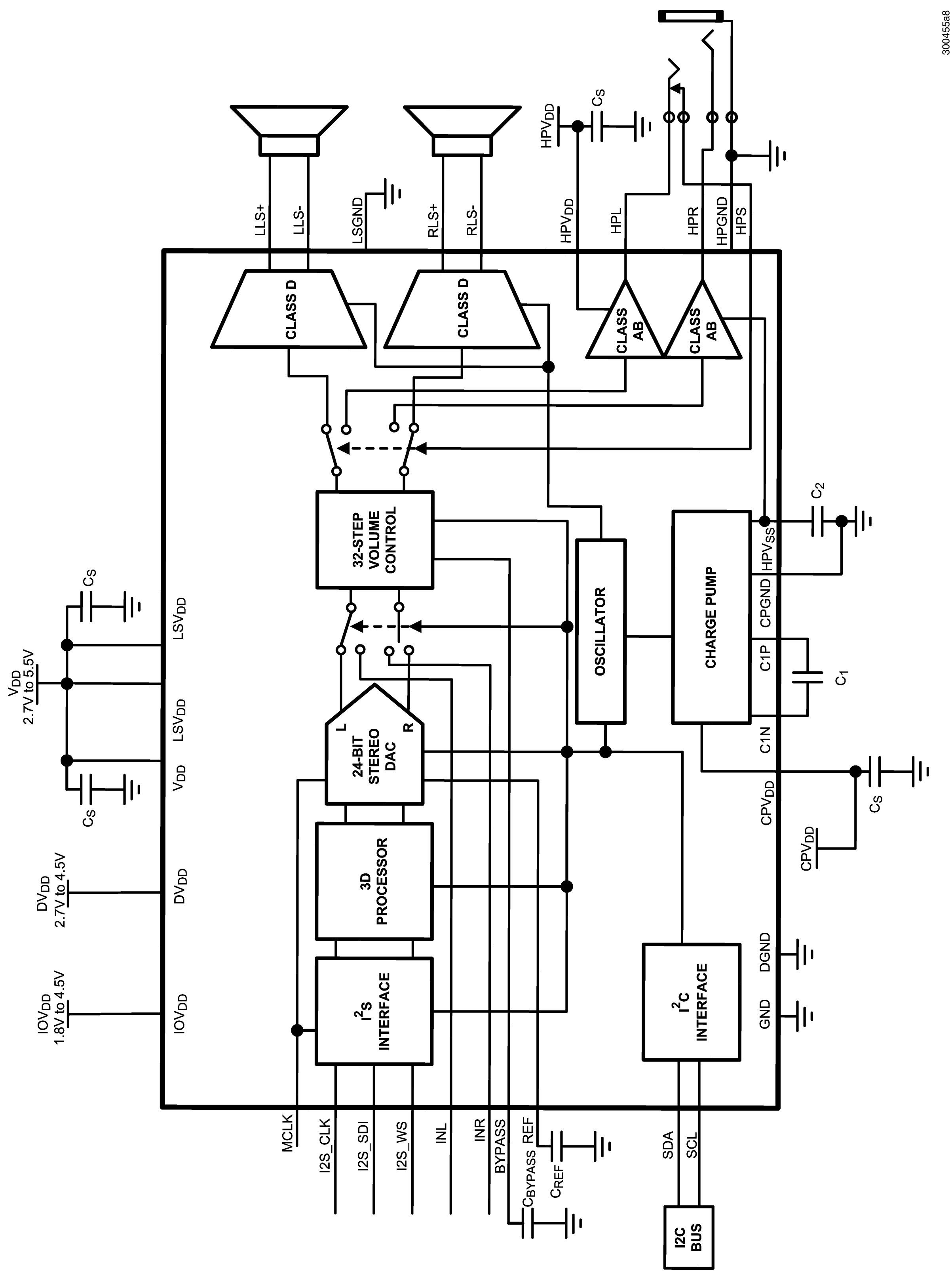
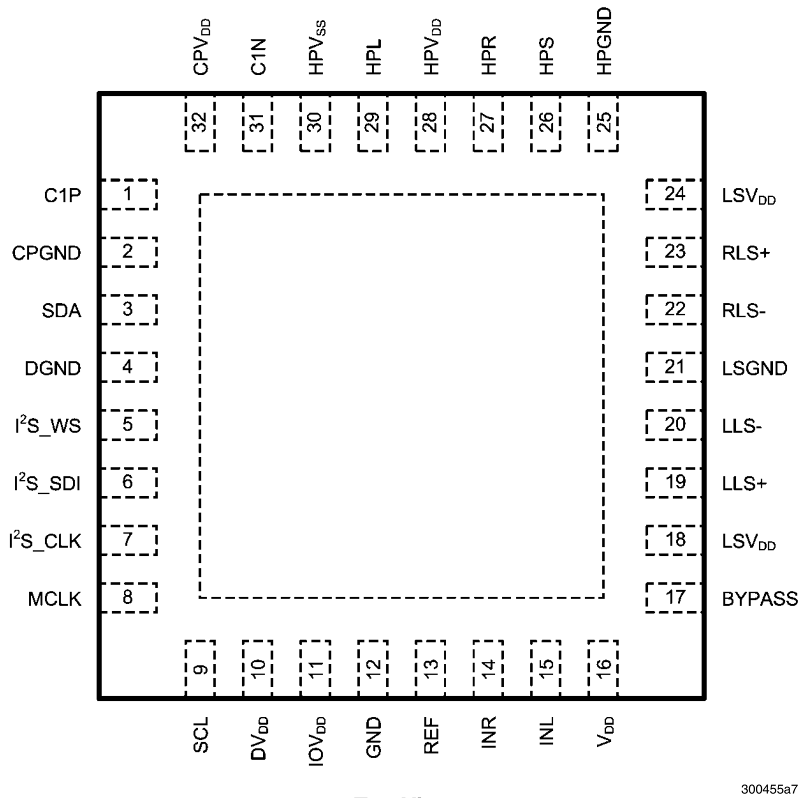


FIGURE 1. Typical Audio Amplifier Application Circuit

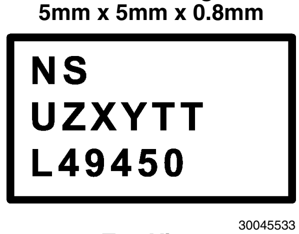
Connection Diagrams

SQ Package
5mm x 5mm x 0.8mm



Top View
Order Number LM49450SQ
See NS Package Number SQA32A

SQ Marking
5mm x 5mm x 0.8mm



Top View
NS - NS Logo
U - Wafer Fab Code
Z - Assembly Plant
XY - 2 Digit Date Code
TT - Lot Traceability
L49450 - LM49450SQ

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 1)	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility(Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Thermal Resistance	
θ_{JC}	2.4°C/W
θ_{JA}	28.4°C/W

Operating Ratings (Notes 1, 2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{DD}, LSV_{DD})	$2.7V \le V_{DD} \le 5.5V$
Headphone Supply Voltage (CPV_{DD}, HPV_{DD})	$1.8V \le V_{DD} \le 2.7V$
Digital Core Supply Voltage (DV_{DD})	$2.7V \le DV_{DD} \le 4.5V$
Digital IO Supply Voltage (IOV_{DD})	$1.8V \le IOV_{DD} \le 4.5V$

Electrical Characteristics $V_{DD} = LSV_{DD} = 3.6V$, $HPV_{DD} = CPV_{DD} = 2.5V$ (Notes 2, 8)

The following specifications apply for Headphone: A_V = 0dB, $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, $C_1 = C_2$ = 2.2µF, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49450		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
DI_{DD}	Digital Core Supply Current	DV_{DD} = 2.7V, f_S = 48kHz, f_{MCLK} = 12.28MHz	9	11.2	mA (max)
I_{SD}	Shutdown Supply Current	Digital Current Analog Current	0.03 0.02	1 1	µA (max) µA (max)
SPEAKER AMPLIFIERS (Headphone Amplifiers Disabled, HPS = 0)					
I_{DDLS}	Analog Supply Current	f_S = 48kHz, DAC Active, No Load Line Inputs Active, No Load	9.8 7	13 10	mA (max) mA (max)
V_{OS}	Output Offset Voltage	DAC Active Line Inputs Active	8 8	45	mV (max) mV (max)
P_{OUT}	Output Power	R_L = 4Ω, f = 1kHz THD+N = 1% THD+N = 10%	 1 1.2		 W W
		R_L = 8Ω, f = 1kHz THD+N = 1% THD+N = 10%	 625 725	525	 mW (min) W
THD+N	Total Harmonic Distortion	P_O = 300mW, f = 1kHz, R_L = 8Ω			
		DAC Active	0.06		%
		Line Inputs Active	0.07		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f = 1kHz			
		DAC Active, Internal Reference	59	45	dB (min)
		DAC Active, External Reference	62		dB
		Line Inputs Active	67		dB
η	Efficiency	P_O = 650, f = 1kHz R_L = 8Ω	87		%
Xtalk	Crosstalk	P_O = 500mW, f = 1kHz, R_L = 8Ω			
		DAC Active, Line Inputs Active	81 77		dB dB
		P_O = 500mW, f = 10kHz, R_L = 8Ω			
		DAC Active, Line Inputs Active	60 60		dB dB

Symbol	Parameter	Conditions	LM49450		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
SNR	Signal to Noise Ratio	P_O = 500mW, f = 1kHz, A-weighted			
		DAC Active, Internal Reference	89		dB
		DAC Active, External Reference	92		dB
		Line Inputs Active	90		dB
A_V	Digitally Controlled Gain Level	Maximum Gain Setting, Line Inputs Active	23.6	22.5 24.1	dB (min) dB (max)
		Minimum Gain Setting, Line Inputs Active	–48	–49 –46	dB (min) dB (max)
Mute	Mute Attenuation	Line Inputs Active	–91		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Matching		0.3		dB
ε_{OS}	Output Noise	Input Referred, A-weighted			
		DAC Active, Internal Reference	43.5		μV
		DAC Active, External Reference	45.4		μV
		Line Inputs Active	40		μV
t_{ON}	Turn-On Time		27		ms
t_{OFF}	Turn-Off Time		1		ms
HEADPHONE AMPLIFIERS (Speaker Amplifiers Disabled, HPS = 1)					
I_{DDHP}	Analog Supply Current	f_S = 48kHz, DAC active Line Inputs Active	7.2 5.3	8.25 6.5	mA (max) mA (max)
V_{OS}	Output Offset Voltage	DAC active, A_V = –6dB Line Inputs Active, , A_V = –6dB	7 5	30	mV mV (max)
P_O	Output Power	R_L = 16Ω, f = 1kHz			
		THD+N = 1%, Single Channel	66		mW
		THD+N = 1%, Two Channels in Phase	34		mW
		R_L = 32Ω, f = 1kHz			
		THD+N = 1%, Single Channel	49	42	mW (min)
		THD+N = 1%, Two Channels in Phase	36	27	mW (min)
THD+N	Total Harmonic Distortion	f = 1kHz, DAC Active			
		R_L = 16Ω, P_O = 5mW	0.05		%
		R_L = 32Ω, P_O = 5mW	0.03		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f = 1kHz			
		DAC Active, Internal Reference	71.2	56	dB (min)
		DAC Active, External Reference	71.3		dB
		Line Inputs Active	76.9		dB
Xtalk	Crosstalk	P_O = 5mW, f = 1kHz, R_L = 32Ω			
		DAC Active, Line Inputs Active	82 79		dB dB
		P_O = 5mW, f = 10kHz, R_L = 32Ω			
		DAC Active, Line Inputs Active	78 76		dB dB
SNR	Signal to Noise Ratio	P_O = 5mW, f = 1kHz, A-weighted			
		DAC Active, Internal Reference	99		dB
		DAC Active, External Reference	102		dB
		Line Inputs Active	98		dB

Symbol	Parameter	Conditions	LM49450 Typical (Note 6)	LM49450 Limit (Note 7)	Units (Limits)
A_V	Digitally Controlled Gain Level	Maximum Gain Setting, Line Inputs Active	17.8	17.0 18.5	dB (min) dB (max)
		Minimum Gain Setting, Line Inputs Active	–53.8	–56 –52	dB (min) dB (max)
Mute	Mute Attenuation	Line Inputs Active	–102		dB
$\Delta A_{CH\text{-}CH}$	Channel-to-Channel Gain Matching		0.3		dB
ε_{OS}	Output Noise	Input Referred, A-weighted			
		DAC Active, Internal Reference	10		μV
		DAC Active, External Reference	10		μV
		Line Inputs Active	10		μV
V_{OUT_FS}	Full-Scale Headphone Amplifier Output Voltage	R_L = No Load	942	850	mV_{RMS} (min)
t_{ON}	Turn-On Time		27		ms
t_{OFF}	Turn-Off Time		1		ms
HEADPHONE SENSE INPUT (HPS)					
V_{IH}	Input High Voltage		1		V
V_{IL}	Input Low Voltage		0.6		V
DIGITAL INTERFACE					
V_{IH}	Input High Voltage			2.8	V (min)
V_{IL}	Input Low Voltage			0.8	V (max)
V_{OH}	Output High Voltage			2	V (min)
V_{OL}	Output Low Voltage			1	V (max)

Electrical Characteristics $V_{DD} = LSV_{DD} = 5.0V$

(Notes 2, 8) The following specifications apply for Headphone: A_V = 0dB, $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49450 Typical (Note 6)	LM49450 Limit (Note 7)	Units (Limits)
SPEAKER AMPLIFIERS (Headphone Amplifiers Disabled, HPS = 0)					
I_{DDLS}	Analog Supply Current	f_S = 48kHz, DAC Active Line Inputs Active	14 10.4	18 16	mA (max) mA (max)
V_{OS}	Output Offset Voltage	DAC Voltage AV = 0dB, Line Inputs Active	15 12	50 48	mV (max) mV (max)
P_{OUT}	Output Power	R_L = 4Ω, f = 1kHz THD+N = 1% THD+N = 10%	 1.9 2.5		 W W
		R_L = 8Ω, f = 1kHz THD+N = 1% THD+N = 10%	 1.25 1.54		 mW (min) W
THD+N	Total Harmonic Distortion	P_O = 635mW, f = 1kHz, R_L = 8Ω			
		DAC Active	0.06		%
		Line Inputs Active	0.04		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f = 1kHz			
		DAC Active, Internal Reference	60		dB
		DAC Active, External Reference	60		dB
		Line Inputs Active	70		dB

Symbol	Parameter	Conditions	LM49450 Typical (Note 6)	LM49450 Limit (Note 7)	Units (Limits)
η	Efficiency	P_O = TBDmW, f = 1kHz R_L = 8Ω	80		%
Xtalk	Crosstalk	P_O = 500mW, f = 1kHz, R_L = 8Ω			
		DAC Active, Line Inputs Active	74 79		dB dB
		P_O = 500mW, f = 10kHz, R_L = 8Ω			
		DAC Active, Line Inputs Active	60 60		dB dB
SNR	Signal to Noise Ratio	P_O = 500mW, f = 1kHz, A-weighted			
		DAC Active, Internal Reference	88		dB
		DAC Active, External Reference	89		dB
		Line Inputs Active	98		dB
A_V	Digitally Controlled Gain Level	Maximum Gain Setting, Line Inputs Active	24.2	22.5 24.2	dB (min) dB (max)
		Minimum Gain Setting, Line Inputs Active	–48	–49 –46	dB (min) dB (max)
Mute	Mute Attenuation	Line Inputs Active	–92		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Matching		0.3		dB
ε_{OS}	Output Noise	Input Referred, A-weighted			
		DAC Active, Internal Reference	60		μV
		DAC Active, External Reference	85		μV
		Line Inputs Active	40		μV
t_{ON}	Turn-On Time		27		ms
t_{OFF}	Turn-Off Time		1		ms

Timing Characteristics

(Notes 2, 8) The following specifications apply for Headphone: A_V = 0dB, $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49450 Typical (Note 6)	LM49450 Limit (Note 7)	Units (Limits)
AUDIO INTERFACE TIMING					
t_{MCLKL}	MCLK Pulse Width Low			16	ns (min)
t_{MCLKH}	MCLK Pulse Width High			16	ns (min)
t_{MCLKY}	MCLK Period			32	ns (min)
t_{BCLKR}	BCLK Rise Time			3	ns (max)
t_{BCLKCF}	BCLK Fall Time			3	ns (max)
t_{BCLKDS}	BCLK Duty Cycle		50		%
t_{DL}	LRC Propagation Delay from BCLK falling edge			10	ns (max)
t_{DST}	DATA Setup Time to BCLK Rising Edge			10	ns (min)
t_{DHT}	DATA Hold Time from BCLK Rising Edge			10	ns (min)
CONTROL INTERFACE TIMING					
	SCLK Frequency			400	kHz (max)
1	Hold Time (repeated START Condition)			0.6	μs (min)

Symbol	Parameter	Conditions	LM49450		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
2	Clock Low Time			1.3	μs (min)
3	Clock High Time			600	ns (min)
4	Setup Time for a Repeated START Condition			600	ns (min)
5	Data Hold Time	Output		300	ns (min)
		Input		0 900	ns (min) ns (max)
6	Data Setup Time			100	ns (min)
7	Rise Time of SDA and SCL			$20+0.1C_B$ 300	ns (min) ns (max)
8	Fall Time of SDA and SCL			$15+0.1C_B$ 300	ns (min) ns (max)
9	Setup Time for STOP Condition			600	ns (min)
10	Bus Free time Between a STOP and START Condition			1.3	μs (min)
C_B	Bus Capacitance			10 200	pF (min) pF (max)

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A= +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: RL is a resistive load in series with two inductors to simulate an actual speaker load. For R_L = 8Ω, the load is 15μH + 8Ω, +15μH. For RL = 4Ω, the load is 15μH + 4Ω + 15μH.

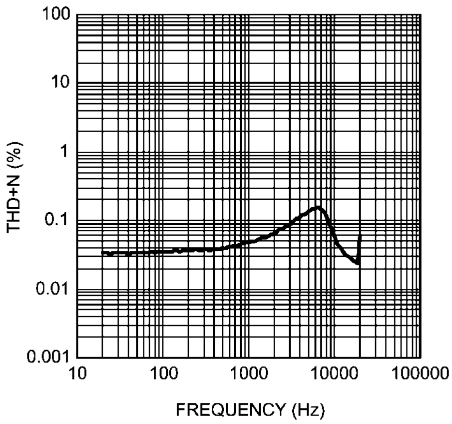
Pin Descriptions

TABLE 1.

Pin	Name	Description
1	C1P	Charge Pump Flying Capacitor Positive Terminal
2	CPGND	Charge Pump Ground
3	SDA	I^2C Serial Data Input
4	DGND	Digital Ground
5	I^2S_WS	I^2S Word Select Input
6	I^2S_SDI	I^2S Serial Data Input
7	I^2S_CLK	I^2S Clock Input
8	MCLK	Master Clock
9	SCL	I2C Clock Input
10	DV_{DD}	Digital Core Power Supply
11	IOV_{DD}	Digital Interface Power Supply
12	GND	Analog Ground
13	REF	DAC Reference Bypass
14	INR	Right Channel Analog Input
15	INL	Left Channel Analog Input
16	V_{DD}	Analog Power Supply
17	BYPASS	Mid-Rail Bias Bypass
18, 24	LSV_{DD}	Speaker Power Supply
19	LLS+	Left Channel Non-Inverting Speaker Output
20	LLS-	Left Channel Inverting Speaker Output
21	LSGND	Speaker Ground
22	RLS-	Right Channel Inverting Speaker Output
23	RLS+	Right Channel Non-Inverting Speaker Output
25	HPGND	Headphone Amplifier Ground
26	HPS	Headphone Sense Input
27	HPR	Right Channel Headphone Amplifier Output
28	HPV_{DD}	Headphone Amplifier Power Supply
29	HPL	Left Channel Headphone Amplifier Output
30	HPV_{SS}	Charge Pump Output and Headphone Amplifier Negative Power Supply.
31	C1N	Charge Pump Flying Capacitor Negative Terminal
32	CPV_{DD}	Charge Pump Power Supply

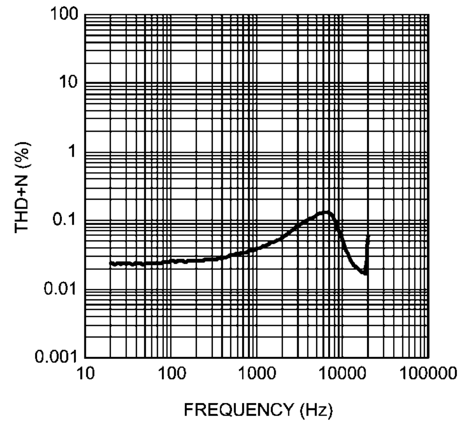
Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 50mW, R_L = 4Ω
DAC Input, Internal Reference, Speaker Mode



300455b6

THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 150mW, R_L = 8Ω
DAC Input, Internal Reference, Speaker Mode



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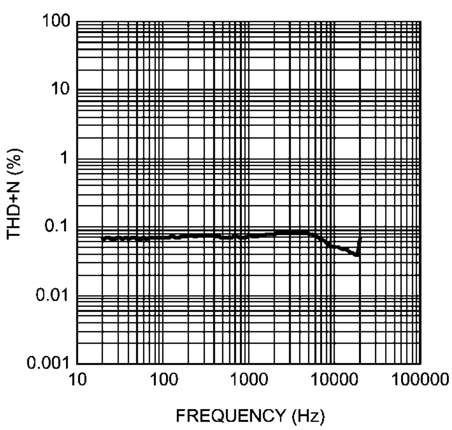
THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 50mW, R_L = 4Ω
DAC Input, External Reference, Speaker Mode



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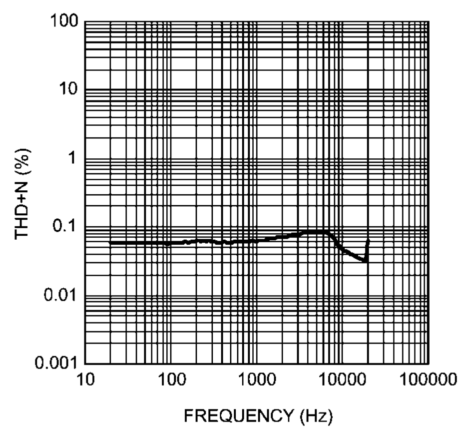
THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 150mW, R_L = 8Ω
DAC Input, External Reference, Speaker Mode



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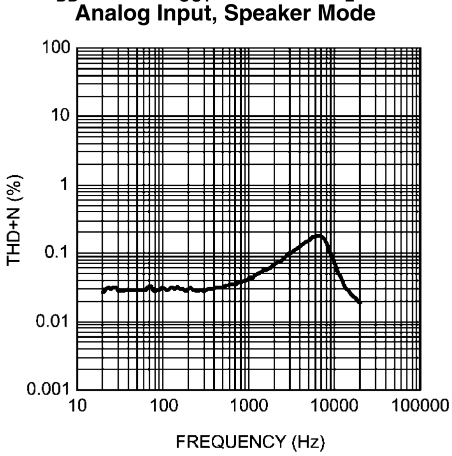
THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 100mW, R_L = 4Ω
Analog Input, Speaker Mode



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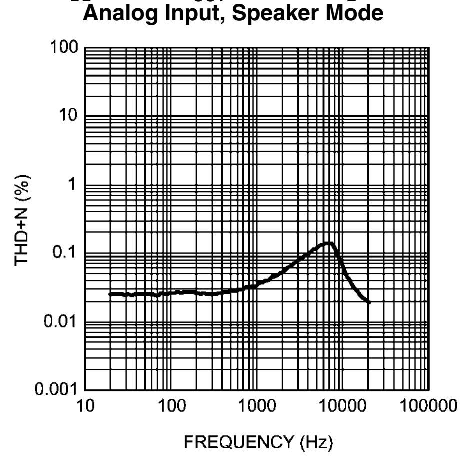
THD+N vs Frequency
V_{DD} = 3.0V, P_{OUT} = 80mW, R_L = 8Ω
Analog Input, Speaker Mode



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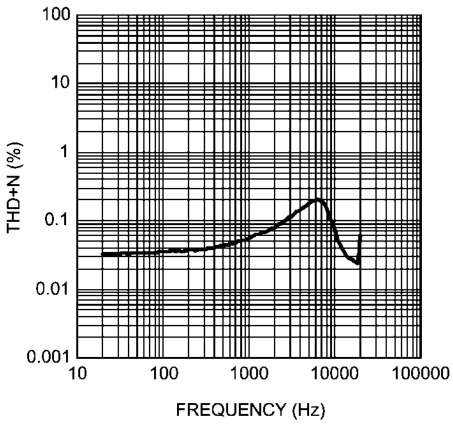
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 100mW, R_L = 4Ω
DAC Input, Internal Reference, Speaker Mode



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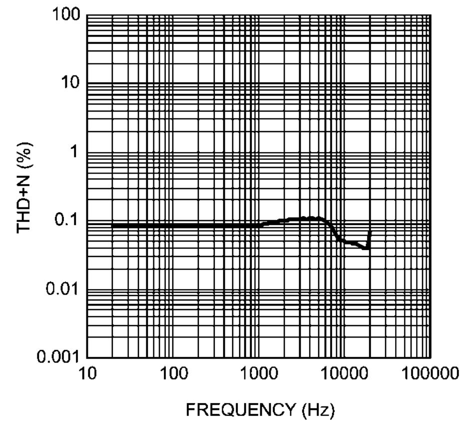
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 100mW, R_L = 4Ω
DAC Input, External Reference, Speaker Mode



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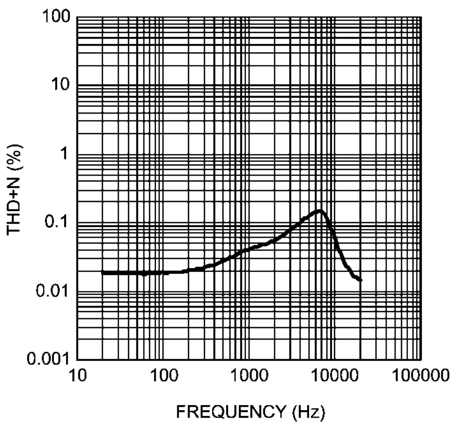
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 100mW, R_L = 8Ω
Analog Input, Speaker Mode



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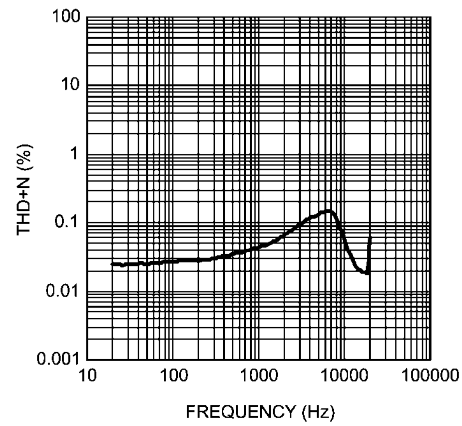
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 200mW, R_L = 8Ω
DAC Input, Internal Reference, Speaker Mode



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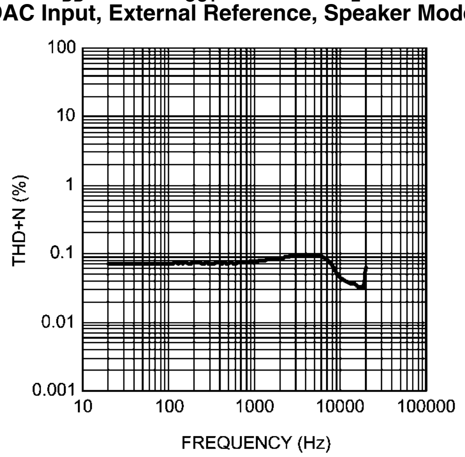
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 200mW, R_L = 8Ω
DAC Input, External Reference, Speaker Mode



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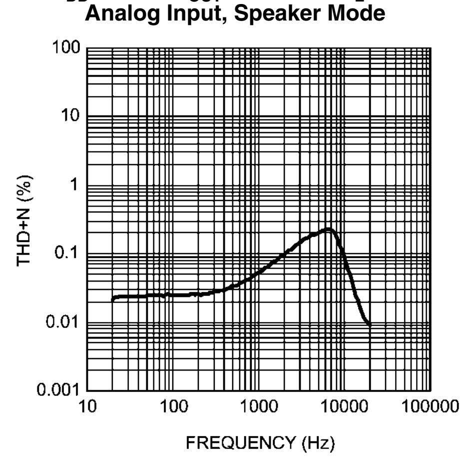
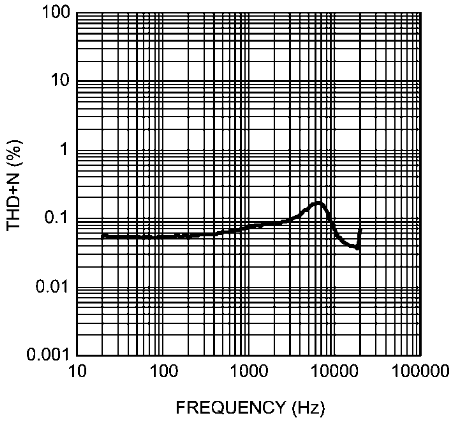
THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 100mW, R_L = 4Ω
Analog Input, Speaker Mode



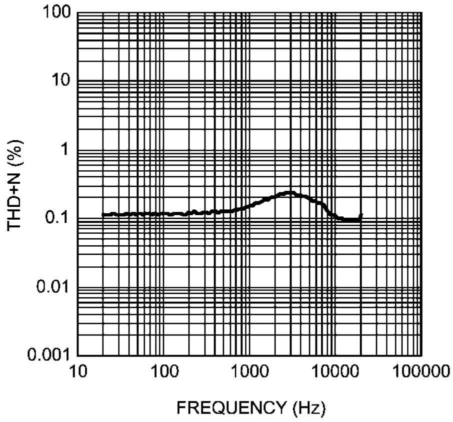
300455d3

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 750mW, R_L = 4Ω
DAC Input, Internal Reference, Speaker Mode



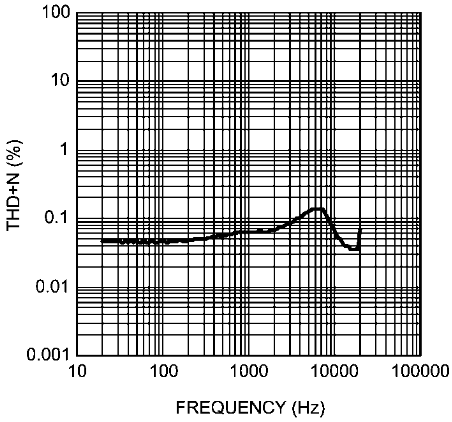
300455b8

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 750mW, R_L = 4Ω
DAC Input, External Reference, Speaker Mode



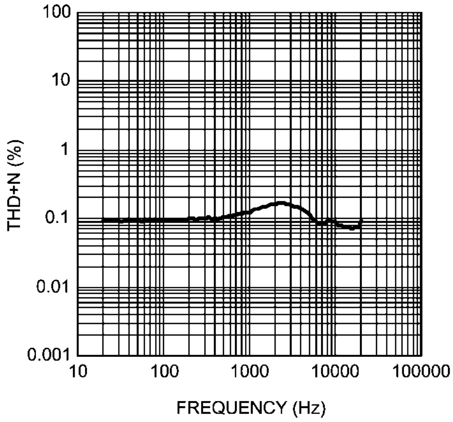
300455c6

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 800mW, R_L = 8Ω
DAC Input, Internal Reference, Speaker Mode



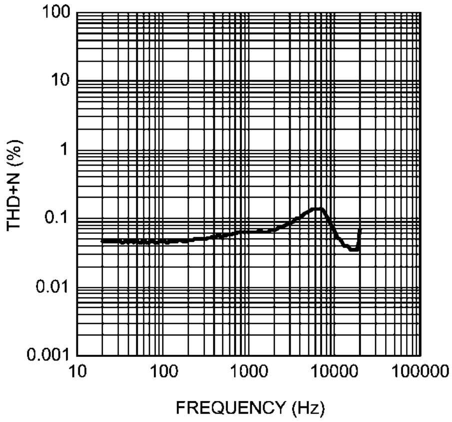
300455c1

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 800mW, R_L = 8Ω
DAC Input, External Reference, Speaker Mode



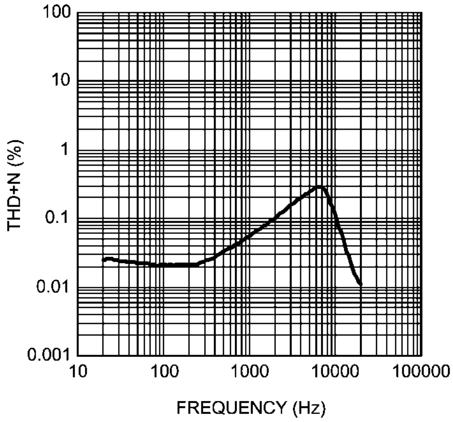
300455c9

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 700mW, R_L = 8Ω
Analog Input, Speaker Mode



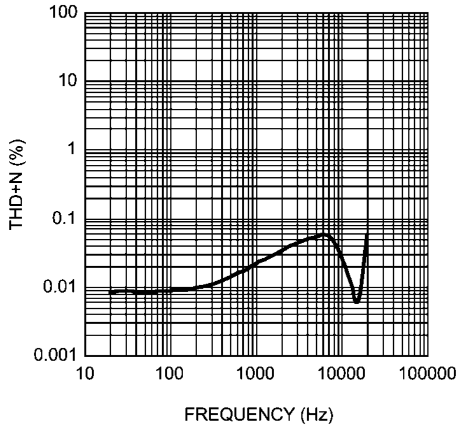
300455d7

THD+N vs Frequency
V_{DD} = 5.0V, P_{OUT} = 1.0W, R_L = 4Ω
Analog Input, Speaker Mode



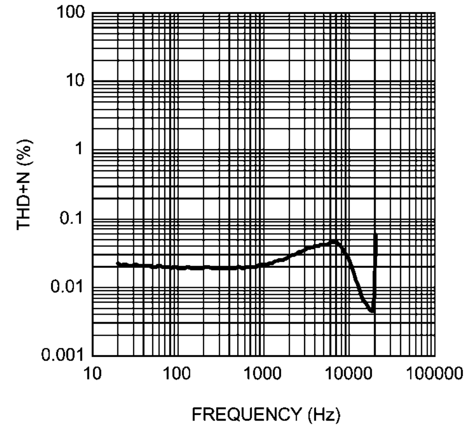
300455d4

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 10mW, R_L = 16Ω
DAC Input, Internal Reference, Headphone Mode



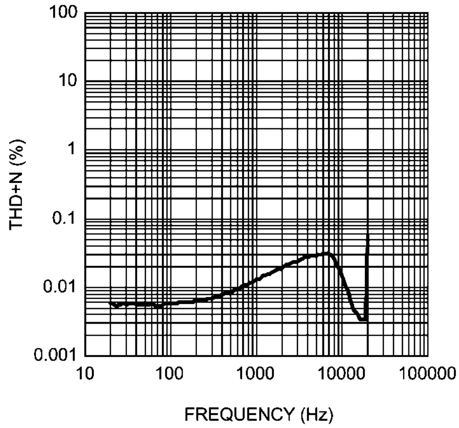
300455f2

THD+N vs Frequency
HPV_{DD} = 2.5V, P_{OUT} = 25mW, R_L = 16Ω
DAC Input, Internal Reference, Headphone Mode



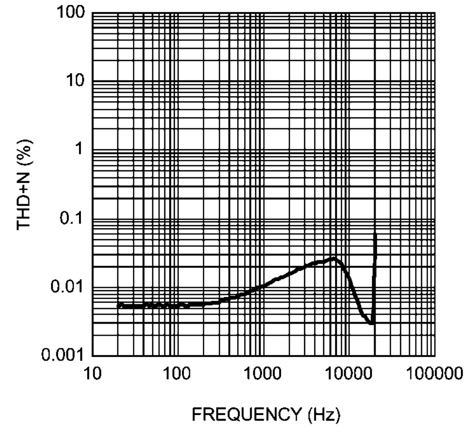
300455f3

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 15mW, R_L = 32Ω
DAC Input, Internal Reference, Headphone Mode



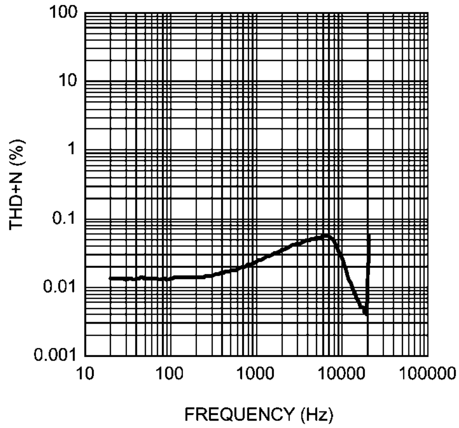
300455f4

THD+N vs Frequency
HPV_{DD} = 2.5V, P_{OUT} = 25mW, R_L = 32Ω
DAC Input, Internal Reference, Headphone Mode



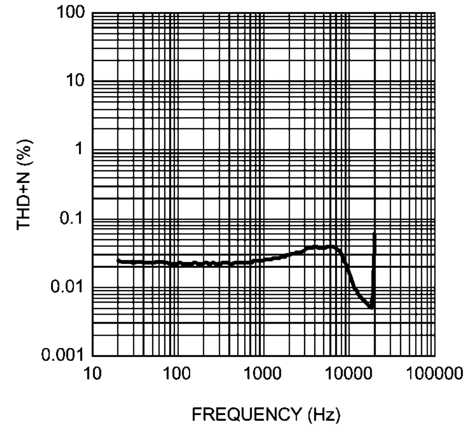
300455f5

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 10mW, R_L = 16Ω
DAC Input, External Reference, Headphone Mode



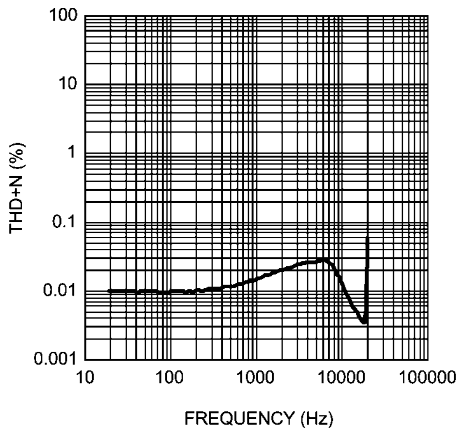
300455f8

THD+N vs Frequency
HPV_{DD} = 2.5V, P_{OUT} = 25mW, R_L = 16Ω
DAC Input, External Reference, Headphone Mode



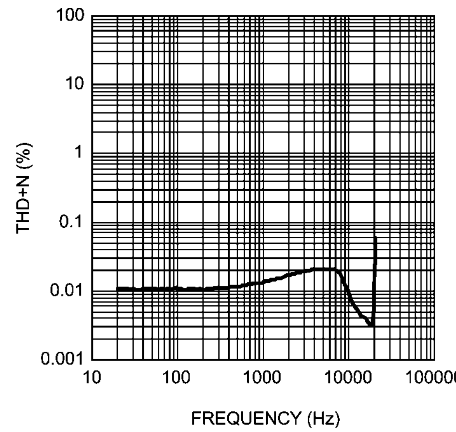
300455f9

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 15mW, R_L = 32Ω
DAC Input, External Reference, Headphone Mode



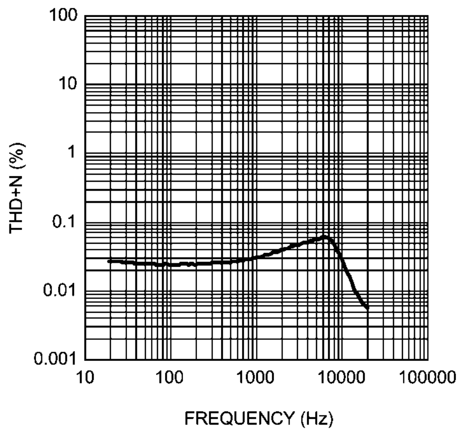
300455g0

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 25mW, R_L = 32Ω
DAC Input, External Reference, Headphone Mode



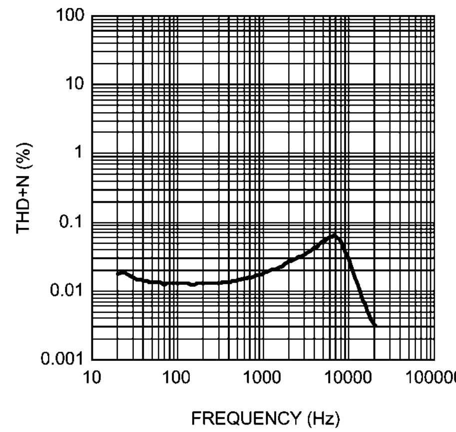
300455g1

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 10mW, R_L = 16Ω
Analog Input, Headphone Mode



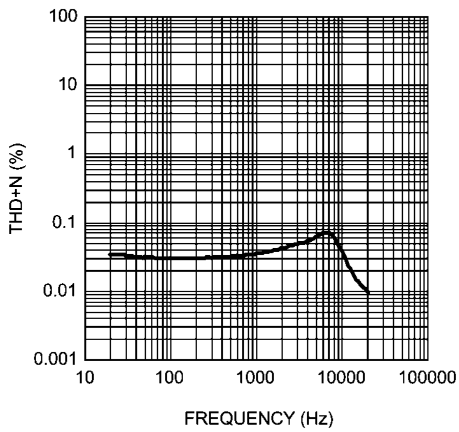
300455g7

THD+N vs Frequency
HPV_{DD} = 2.0V, P_{OUT} = 10mW, R_L = 32Ω
Analog Input, Headphone Mode



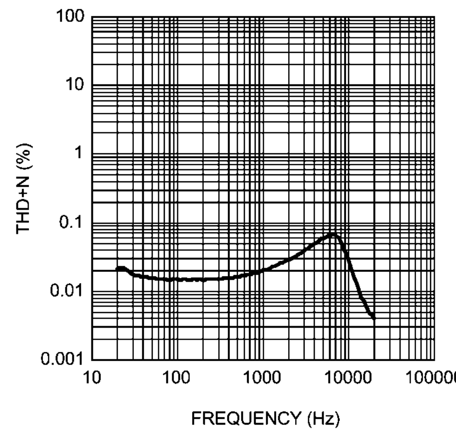
300455g9

THD+N vs Frequency
HPV_{DD} = 2.5V, P_{OUT} = 15mW, R_L = 16Ω
Analog Input, Headphone Mode



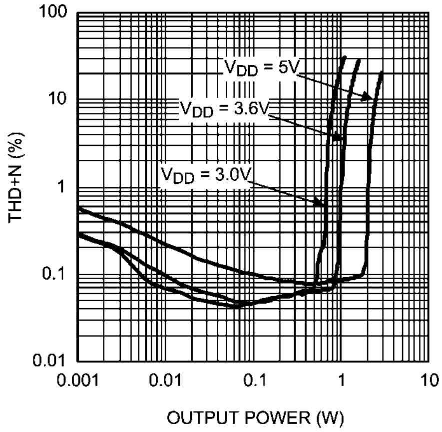
300455g8

THD+N vs Frequency
HPV_{DD} = 2.5V, P_{OUT} = 15mW, R_L = 32Ω
Analog Input, Headphone Mode



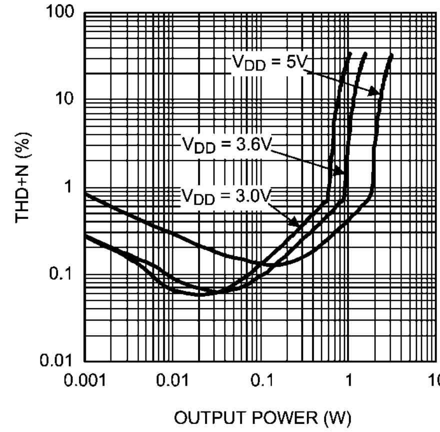
300455h0

THD+N vs Output Power
A_V = 12dB, R_L = 4Ω, f = 1kHz
DAC Input, Internal Reference, Speaker Mode



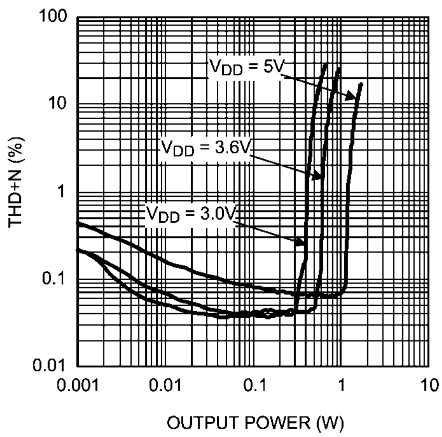
300455b4

THD+N vs Output Power
A_V = 12dB, R_L = 4Ω, f = 1kHz
DAC Input, External Reference, Speaker Mode



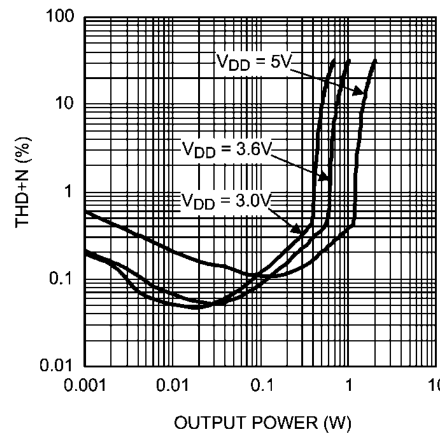
300455c2

THD+N vs Output Power
A_V = 12dB, R_L = 8Ω, f = 1kHz
DAC Input, Internal Reference, Speaker Mode



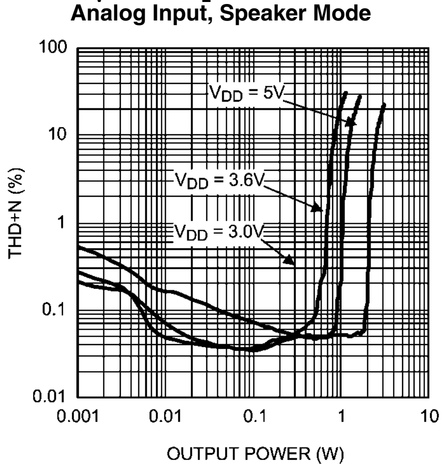
300455b5

THD+N vs Output Power
A_V = 12dB, R_L = 8Ω, f = 1kHz
DAC Input, External Reference, Speaker Mode



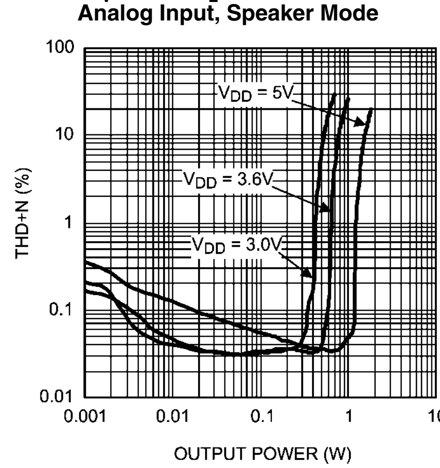
300455c3

THD+N vs Output Power
A_V = 6dB, R_L = 4Ω, f = 1kHz
Analog Input, Speaker Mode



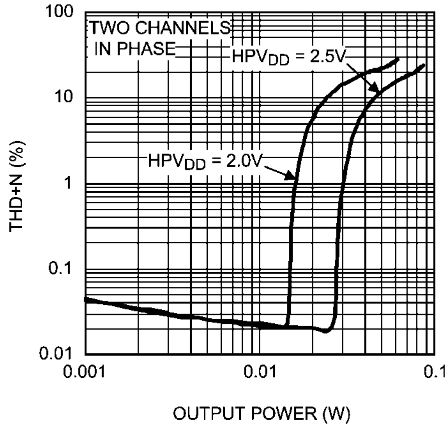
300455d0

THD+N vs Output Power
A_V = 6dB, R_L = 8Ω, f = 1kHz
Analog Input, Speaker Mode



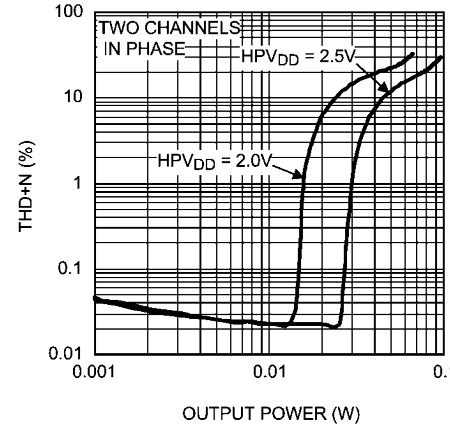
300455d1

THD+N vs Output Power
A_V = 9dB, R_L = 16Ω, f = 1kHz
DAC Input, Internal Reference, Headphone Mode



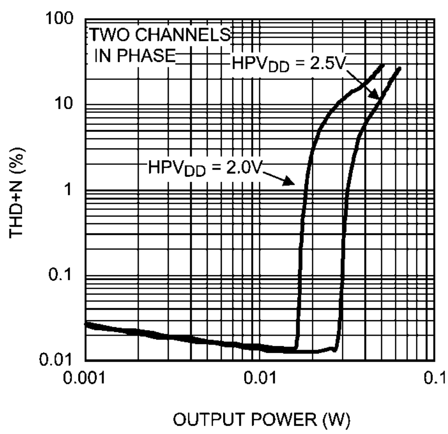
300455f0

THD+N vs Output Power
A_V = 9dB, R_L = 16Ω, f = 1kHz
DAC Input, External Reference, Headphone Mode



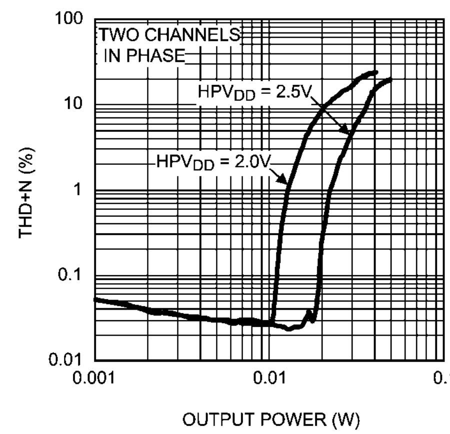
300455f6

THD+N vs Output Power
A_V = 9dB, R_L = 32Ω, f = 1kHz
DAC Input, External Reference, Headphone Mode



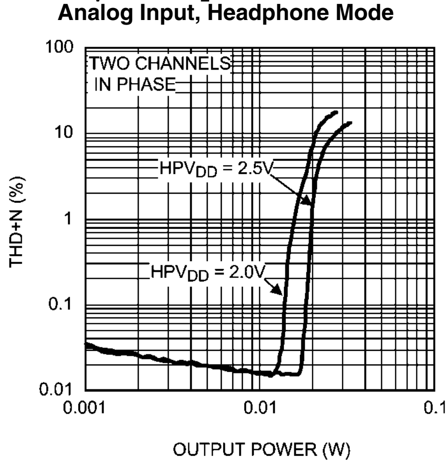
300455f7

THD+N vs Output Power
A_V = 0dB, R_L = 16Ω, f = 1kHz
Analog Input, Headphone Mode



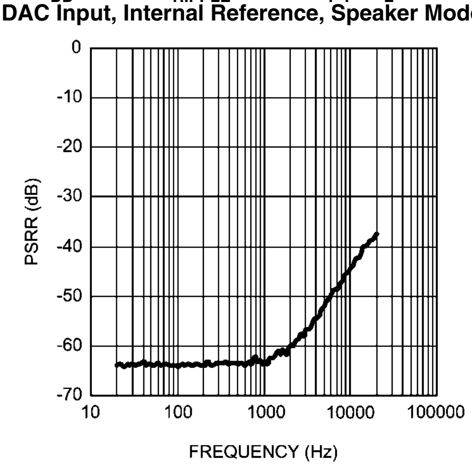
300455g5

THD+N vs Output Power
A_V = 0dB, R_L = 32Ω, f = 1kHz
Analog Input, Headphone Mode



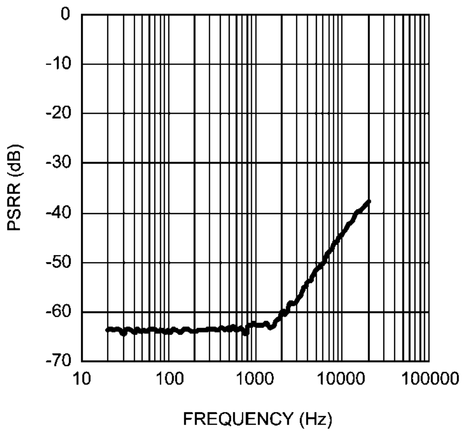
300455g6

PSRR vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
DAC Input, Internal Reference, Speaker Mode



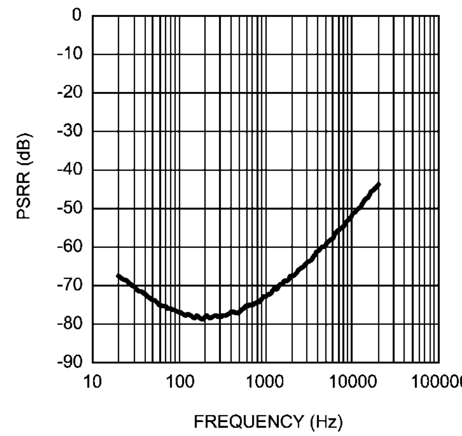
300455e4

PSRR vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
DAC Input, External Reference, Speaker Mode



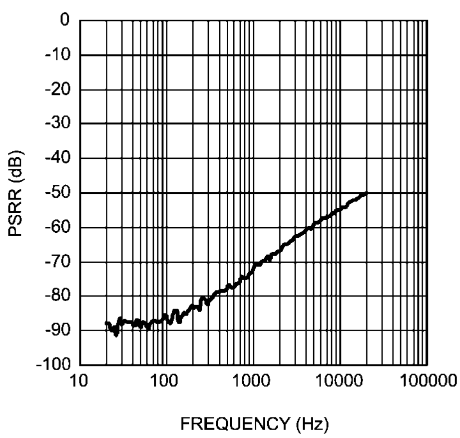
300455e5

PSRR vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω
Analog Input, Speaker Mode



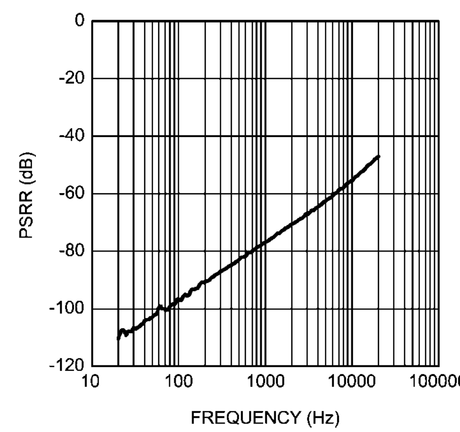
300455e7

PSRR vs Frequency
HPV_{DD} = 2.5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
DAC Input, Internal Reference, Headphone Mode



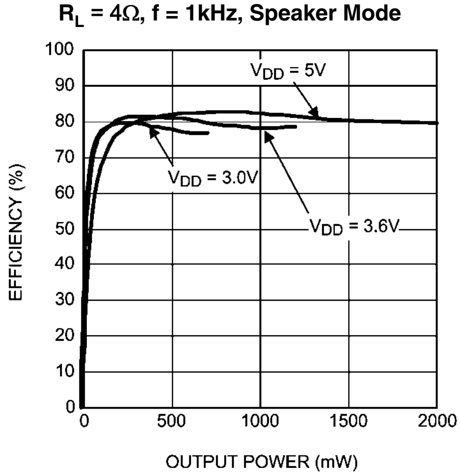
300455g2

PSRR vs Frequency
HPV_{DD} = 2.5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω
Analog Input, Headphone Mode



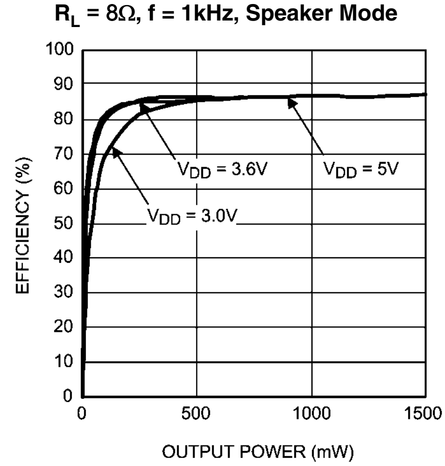
300455h5

Efficiency vs Output Power
R_L = 4Ω, f = 1kHz, Speaker Mode



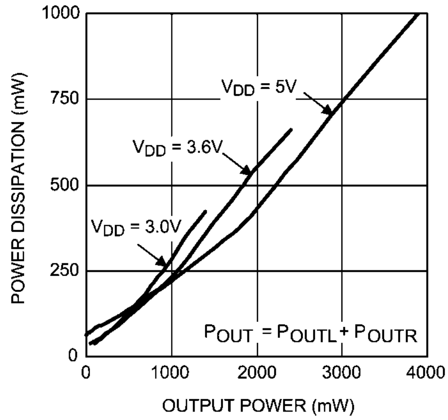
300455d8

Efficiency vs Output Power
R_L = 8Ω, f = 1kHz, Speaker Mode



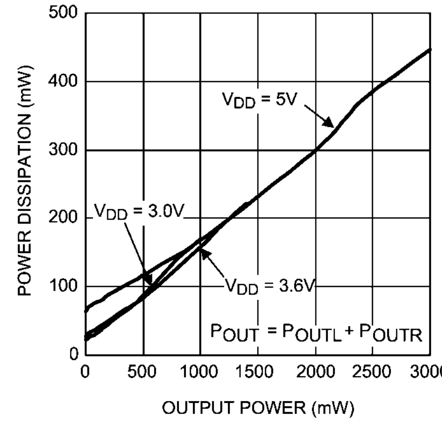
30045520

Power Dissipation vs Output Power
R_L = 4Ω, f = 1kHz, Speaker Mode



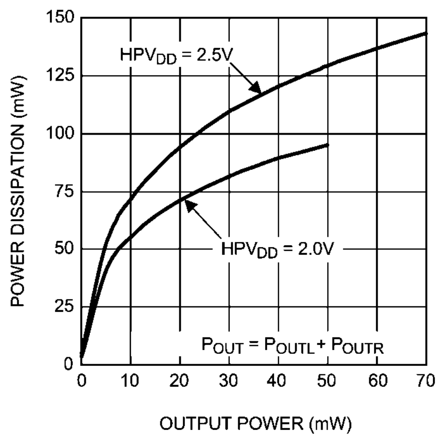
300455e0

Power Dissipation vs Output Power
R_L = 8Ω, f = 1kHz, Speaker Mode



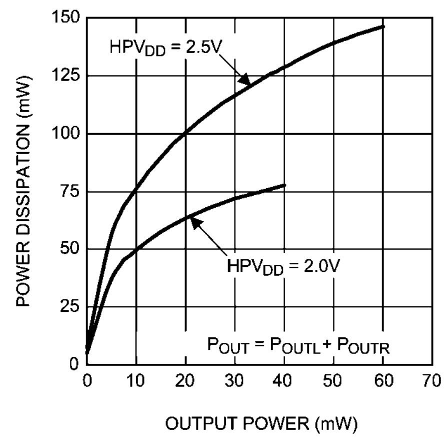
300455e1

Power Dissipation vs Output Power
R_L = 16Ω, f = 1kHz, Headphone Mode



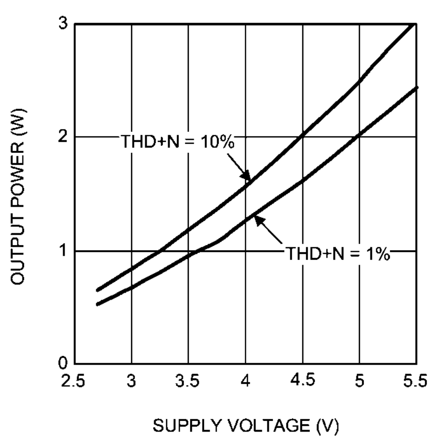
300455h1

Power Dissipation vs Output Power
R_L = 32Ω, f = 1kHz, Headphone Mode



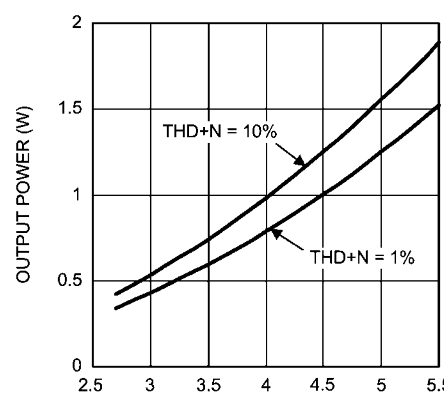
300455h2

Output Power vs Supply Voltage
R_L = 4Ω, f = 1kHz, Speaker Mode



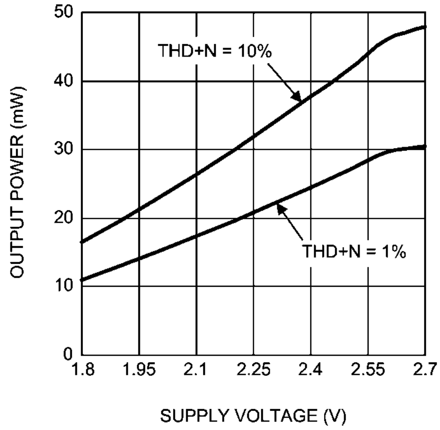
300455e2

Output Power vs Supply Voltage
R_L = 8Ω, f = 1kHz, Speaker Mode



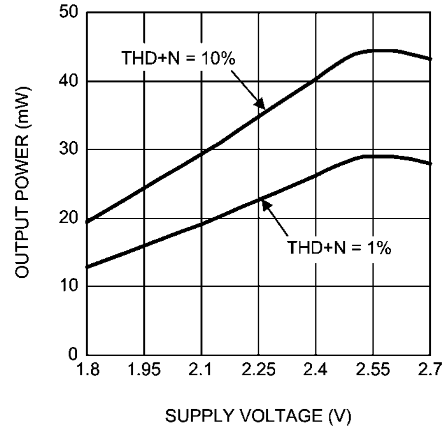
300455e3

Output Power vs Supply Voltage
R_L = 16Ω, f = 1kHz, Headphone Mode



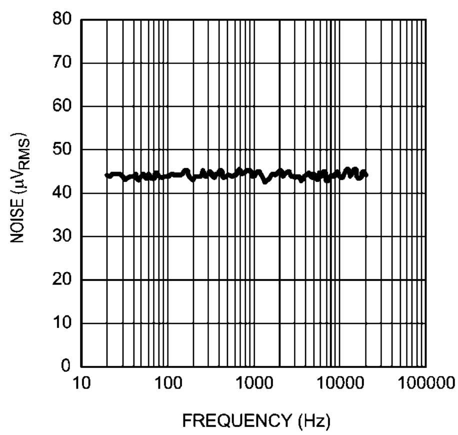
300455h3

Output Power vs Supply Voltage
R_L = 32Ω, f = 1kHz, Headphone Mode



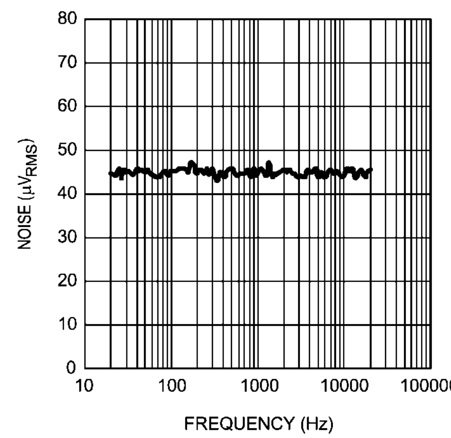
300455h4

Output Noise vs Frequency
V_{DD} = 3.6V, R_L = 8Ω
DAC Input, Internal Reference, Speaker Mode



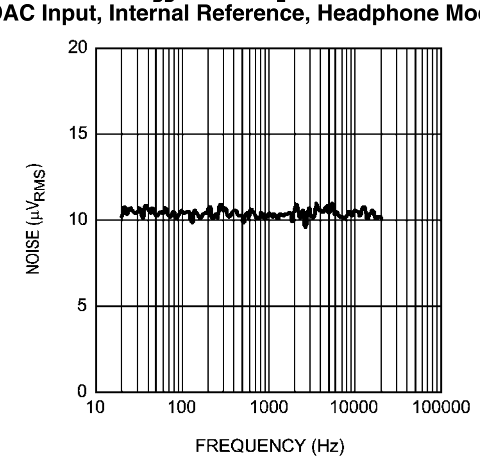
300455e6

Output Noise vs Frequency
V_{DD} = 3.6V, R_L = 8Ω
Analog Input, Speaker Mode



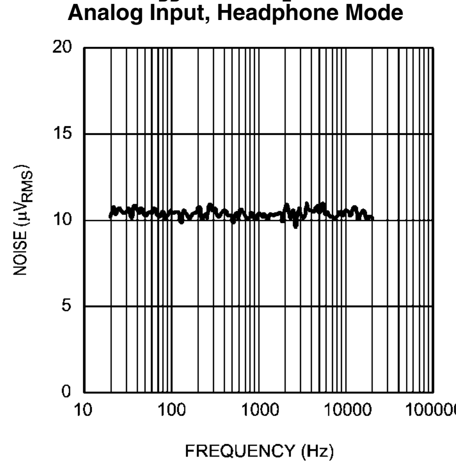
300455e8

Output Noise vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
DAC Input, Internal Reference, Headphone Mode



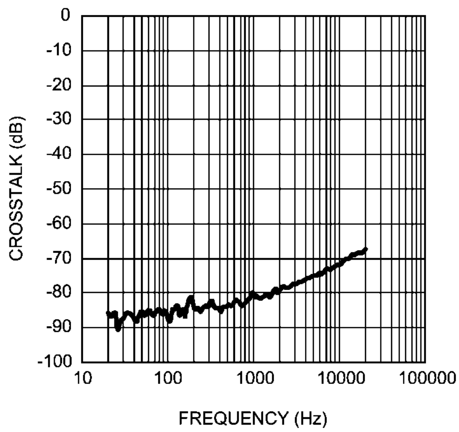
300455g4

Output Noise vs Frequency
HPV_{DD} = 2.5V, R_L = 32Ω
Analog Input, Headphone Mode



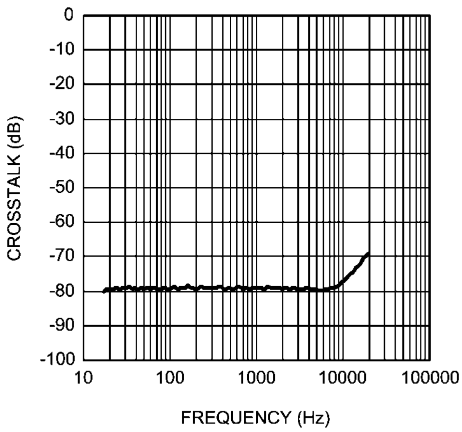
300455h6

Crosstalk vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 1V_{P-P}, R_L = 8Ω
Analog Input, Speaker Mode



300455e9

Crosstalk vs Frequency
V_{DD} = 2.5V, V_{RIPPLE} = 1V_{P-P}, R_L = 8Ω
Analog Input, Headphone Mode



300455h7

Application Information

I2C COMPATIBLE INTERFACE

The LM49450 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open collector). The LM49450 and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49450 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, register address and register data, transmitted over the bus is 8 bits long as is always followed by and acknowledge pulse (Figure 3). The LM49450 device address is 1111101.

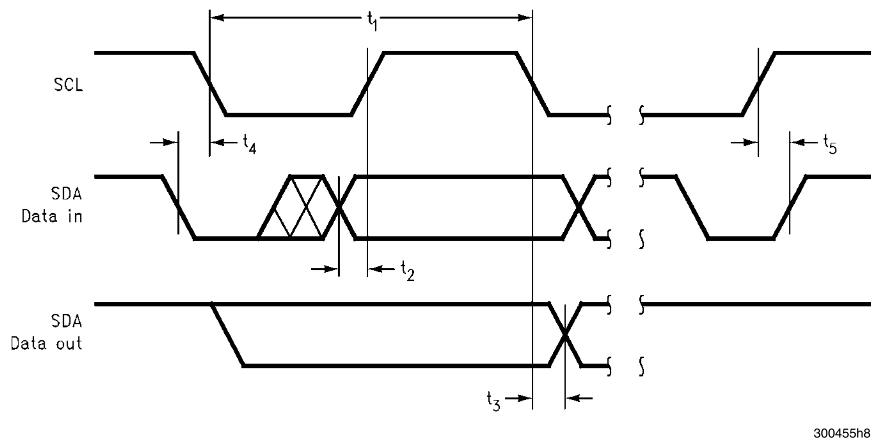


FIGURE 2. I2C Timing Diagram

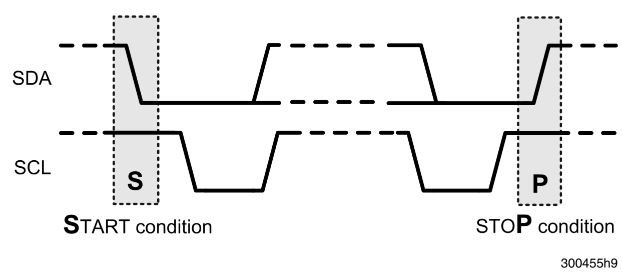


FIGURE 3. START and STOP Diagram

FIGURE 4. Example I2C Write Cycle

BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit (R/$\overline{W}$ = 0 indicates the master is writing to the LM49450, R/$\overline{W}$ = 1 indicates the master wants to read data from the LM49450). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49450 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM49450 sends another ACK bit. Following the acknowledgement of the register address, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data is sent, the LM49450 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SDA is high.

I²S DATA FORMAT

The LM49450 supports three I²S formats: Normal Mode (Figure 5), Left Justified Mode (Figure 6), and Right Justified Mode (Figure 7). In Normal Mode, the audio data is transmitted MSB first, with the unused bits following the LSB. In Left Justified Mode, the audio data format is similar to the Normal Mode, without the delay between the LSB and the change in I²S_WS. In Right Justified Mode, the audio data MSB is transmitted after a delay of a preset number of bits.

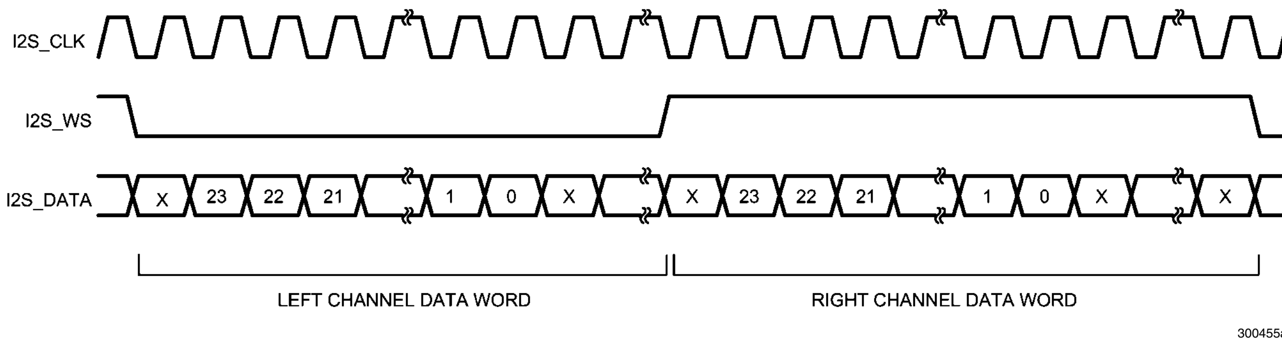


FIGURE 5. I²S Normal Input Format

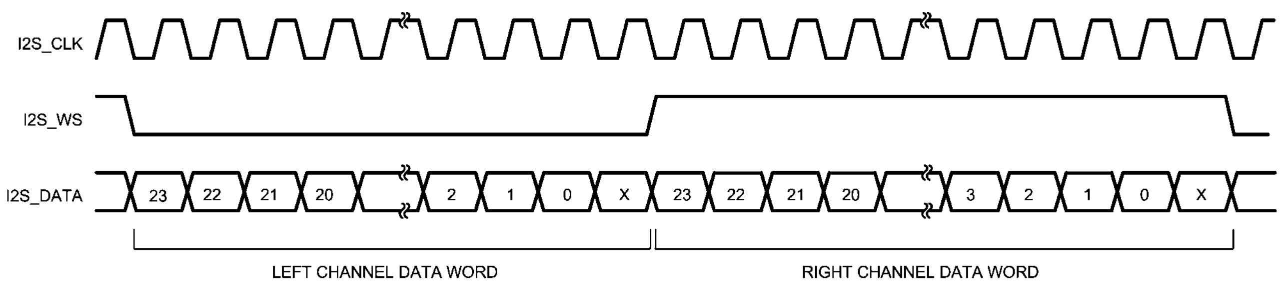


FIGURE 6. I²S Left Justified Input Format

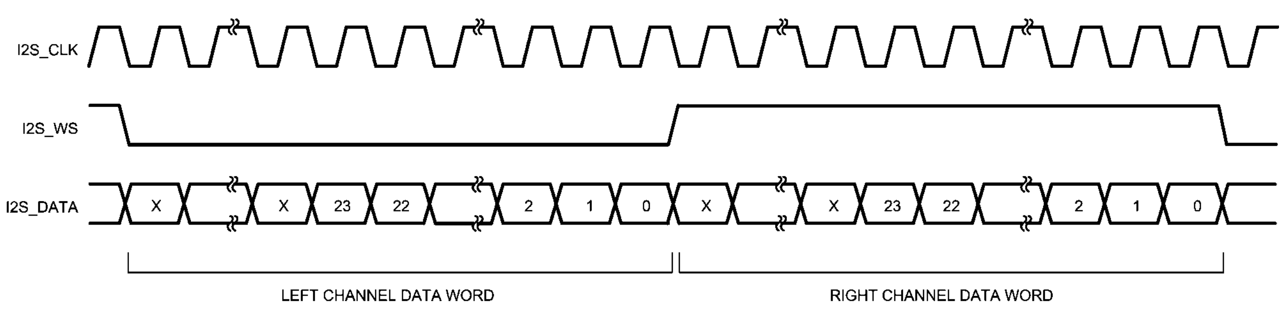


FIGURE 7. I²S Right Justified Input Format

GENERAL AMPLIFIER FUNCTION

Class D Amplifier

The LM49450 features a high-efficiency stereo Class D audio power amplifier that utilizes National's filterless modulation scheme which reduces external component count, conserves board space and reduces system cost. The Class D outputs transition between V_{DD} and GND with a 300kHz switching frequency. With no signal applied, the outputs switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With the input signal applied, the duty cycle (pulse width) of the LM49450 outputs changes. For increasing output voltage, the duty cycle of V_LS+ increases while the duty cycle of V_LS- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yield the differential output voltage.

Fixed Frequency Mode

The LM49450 features two modulation schemes, a fixed frequency mode and a spread spectrum mode. Select the fixed frequency mode by setting the SS bit (B3) in the Mode Control Register (0x00h) to 0. In fixed frequency mode, the speaker amplifier outputs switch at a constant 300kHz. The output spectrum in fixed frequency mode consists of the fundamental and its associated harmonics (see *Typical Performance Characteristics*).

Spread Spectrum

The logic selectable spread spectrum mode eliminates the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM49450 spreads that energy over a larger bandwidth (see Typical Performance Characteristics). The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. Set the SS bit (B3) in the Mode Control Register (0x00h) to 1 to select spread spectrum mode.

Headphone Amplifier

The LM49450 headphone amplifiers feature National's ground referenced architecture that eliminates the large DC-blocking capacitors required at the outputs of traditional headphone amplifiers. A low-noise inverting charge pump creates a negative supply (HPV_{SS}) from the positive supply voltage (CPV_{DD}). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND, instead of a nominal DC voltage (typically $V_{DD}/2$), like traditional amplifiers. Because there is no DC component to the headphone output signals, the large DC-blocking capacitors (typically 220μF) are not necessary, conserving board space and system cost, while improving frequency response.

Power Supplies

The LM49450 uses different power supplies for each portion of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The analog input, and gain (volume control) stages for both speaker and headphones are powered from V_{DD}. The speaker output stage is powered from LSV_{DD}. The headphone amplifiers and charge pump are powered from HPV_{DD}. The separate power supplies allow the class D amplifiers to operate from a higher voltage, maximizing headroom, while the headphones operate from a lower voltage, improving power dissipation, as well as minimizing switching noise coupling between the speaker and headphone amplifiers. The digital portion of the device is powered from DV_{DD}, including the 3D processing core and DAC. IOV_{DD} powers the I^2S and I^2C, allowing the LM49450 to interface with lower voltage digital controllers.

National's 3D Enhancement

The LM49450 digital audio path features National's 3D enhancement that widens or narrows the perceived soundstage of a stereo audio signal. The 3D enhancement either increases or decreases the apparent stereo channel separation, improving audio reproduction whenever the placement of both left and right speakers is not ideal.

The LM49450 3D function is controlled through the I^2C interface. The headphone and speakers have independent 3D controls, allowing each signal path to have its own individual 3D configuration. The LM49450 3D features two effect modes, a narrow effect that decreases the channel separation, making the speakers sound closer together, and a wide effect that makes the speakers sound farther apart. Because the narrow effect mode adds a portion of the left and right signals together, a selectable 6dB attenuation mode is provided to maintain a constant output amplitude when the narrow effect mode is active without changing the volume level. The high pass 3dB roll off frequency, 3D gain (amount channel mixing), and narrow/wide effect selection is done through registers 0x05h (headphone) and 0x06h (speaker. See the *Headphone 3D Configuration Register* and *Loudspeaker 3D Control Register* sections for more information.

Headphone Sense

The LM49450 features a headphone sense input (HPS) that monitors the headphone jack and configures the device depending on the presence of a headphone. When the HPS pin is low, indicating that a headphone is not present, the LM49450 speaker amplifiers are active and the headphone amplifiers are disabled. When the HPS pin is high, indicating that a headphone is present, the headphone amplifiers are active while the speaker amplifiers are disabled.

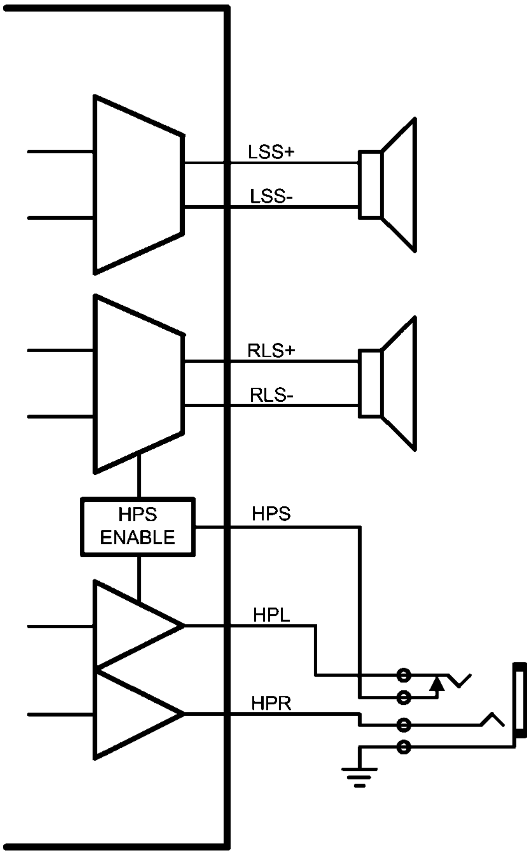


FIGURE 8. HPS Connection

Volume Control

The LM49450 features two separate 32-step volume controls, one for the speaker channels and one for the headphone channels. This allows for the gain of the headphone and speakers to be set independently of each other.

External Reference

The LM49450 can be used with an external reference. Disable the internal reference by setting bit B7 of the Mode Control Register (0x00h) to 1. This allows an external reference voltage to be applied to REF. For proper operation, do not allow the V_{REF} to exceed V_{DD}.

Low Power Shutdown

The LM49450 features an I²C selectable low power shutdown mode that disables the entire device, reducing quiescent current consumption to 0.05μA (digital + analog current). Set bit B0 in the mode control register (0x00h) to 0 to disable the device. Set B0 to 1 to enable the device.

I2S CLOCK CONTROL

The LM49450 features the ability to derive multiple clock signals, including the DAC clock, I²S clock and word select clock in master mode, and the charge pump oscillator frequency, from the MCLK input.

DAC Clock Divider (RDIV)

Bits B5-B0 in the CLOCK CONTROL register (0x01h) are the RDIV bits that set the DAC clock divider ratio. The DAC clock derived from MCLK needs to match the DAC sampling rate. For example, with f_{MCLK} = 12.288MHz and a 64*f_S oversampling ratio (f_S = 48kHz), the DAC requires a 6.144MHz clock. In this case, set the RDIV ratio to divide by 2. In other instances, there may not be a suitable divider ratio for a given sampling rate and MCLK frequency. In this case, f_{MCLK} may need to be altered. See the *Clock Control Register* section for more information.

I²S WS Clock Dividers (I2S_CLK, WS_CLK)

In I²S master mode, the LM49450 I2S CLOCK CONTROL register (0x04h) can be used to set the I²S clock and WS clock frequency. In I2S clock master mode, bits B7-B4 of the I2S CLOCK CONTROL register, the I2S_CLK bits, set the I²S clock divider ratio. The LM49450 derives the I²S clock from DAC clock based on the ratio set by the I2S_CLK bits. The I²S clock is output on I²S_CLK.

In I²S master mode, bits B3 and B2 (I2S_WS) of the I2S CLOCK CONTROL register set the bit length per data word of the I²S WS.

Charge Pump Clock Divider (CPDIV)

The ground referenced headphone amplifiers charge pump derives its clock from MCLK. Bits B7-B0 of the CHARGE PUMP CLOCK register (0x02h) set the charge pump clock divider ratio. See the *Charge Pump Clock Register* section for more information.

CONTROL REGISTERS — Register Map

Register Addess	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00h	MODE CONTROL	EXT_REF	DAC_MODE_1	DAC_MODE_ 0	COMP	SS	MUTE	LINE_IN	ENABLE
0x01h	CLOCK	DAC_DITHER _OFF	DAC_DITHER _ON	RDIV_5	RDIV_4	RDIV_3	RDIV_2	RDIV_1	RDIV_0
0x02h	CHARGE PUMP CLOCK FREQUENCY	CPDIV_7	CPDIV_6	CPDIV_5	CPDIV_4	CPDIV_3	CPDIV_2	CPDIV_1	CPDIV_0
0x03h	I2S MODE	RESERVED	I2S_WRD_2	I2S_WRD_1	I2S_WRD_0	I2S STEREO _REVERSE	I2S_WORD _ORDER	I2S_MODE_1_	I2S_MODE_0
0x04h	I2S CLOCK	I2S_CLK_3	I2S_CLK_2	I2S_CLK_1	I2S_CLK_0	I2S_WS_1	I2S_WS_0	I2S_WS_MS	I2S_CLK_MS
0x05h	HEADPHONE 3D CONTROL	RESERVED	HP_3DATTN	HP_3DFREQ_1	HP_3DFREQ_0	HP_3D_GAIN_1	HP_3D_GAIN_0	HP_3D_MODE	HP_3DEN
0x06h	SPEAKER 3D CONTROL	RESERVED	LS_3DATTN	LS_3DFREQ_1	LS_3DFREQ_0	LS_3DGAIN_1	LS_3DGAIN_0	LS_3D_MODE	LS_3DEN
0x07h	HEADPHONE VOLUME CONTROL	RESERVED	RESERVED	RESERVED	HP4	HP3	HP2	HP1	HP0
0x08h	SPEAKER VOLUME CONTROL	RESERVED	RESERVED	RESERVED	LS4	LS3	LS2	LS1	LS0
0x09h	CMP_0_LSB	C0_7	C0_6	C0_5	C0_4	C0_3	C0_2	C0_1	C0_0
0x0Ah	CMP_0_MSB	C0_15	C0_14	C0_13	C0_12	C0_111	C0_10	C0_09	C0_08
0x0Bh	CMP_1_LSB	C1_7	C1_6	C1_5	C1_4	C1_3	C1_2	C1_1	C1_0
0x0Ch	CMP_1_MSB	C1_15	C1_14	C1_13	C1_12	C1_11	C1_10	C1_09	C1_08
0x0Dh	CMP_2_LSB	C2_7	C2_6	C2_5	C2_4	C2_3	C2_2	C2_1	C2_0
0x0Eh	CMP_2_MSB	C2_15	C2_14	C2_13	C2_12	C2_11	C2_10	C2_09	C2_08

MODE CONTROL REGISTER (0x00h)

Default value is 0x00h.

TABLE 2. Mode Control Register

Bit	Name	Value		Description
B7	EXT_REF	0		Internal reference selected
		1		External reference selected. See External Reference section.
B6:B5	DAC_MODE_1 (B6) DAC_MODE_0 (B5)	B6	B5	Select DAC over sampling Rate
		0	0	125
		0	1	128
		1	0	64
		1	1	32
B4	COMP	0		Default DAC compensation filter selected
		1		Programmable DAC compensation filter selected. See DAC Compensation Filter section.
B3	SS	0		Fixed frequency oscillator selected
		1		Spread spectrum oscillator selected
B2	MUTE	0		Un-mute device
		1		Mute device
B0	ENABLE	0		Device shutdown. Default state during a POR event
		1		Device enabled.

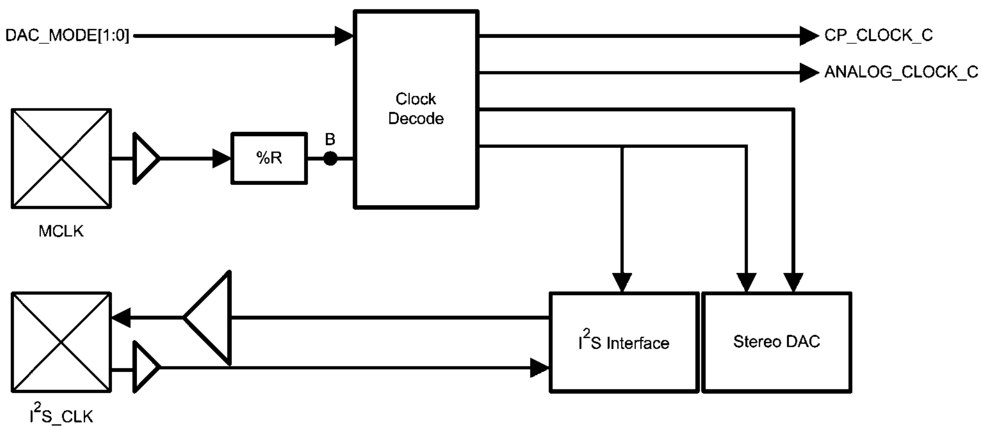
CLOCK CONTROL REGISTER (0x01h)

Default value is 0x00h.

TABLE 3. Clock Control Register

Bit	Name	Value						Description
B7	DAC_DITHER_OFF	0						Default DAC state
		1						Permanently disables DAC dither
B6	DAC_DITHER_ON	0						Default DAC state
		1						Permanently enables DAC dither
B5:B0	RDIV_5 (B5) RDIV_4 (B4) RDIV_3 (B3) RDIV_2 (B2) RDIV_1 (B1) RDIV_0 (B0)	B5	B4	B3	B2	B1	B0	Sets MCLK divider ratio
		0	0	0	0	0	0	Bypass divider
		0	0	0	0	0	1	1
		0	0	0	0	1	0	1.5
		0	0	0	0	1	1	2
		0	0	0	1	0	0	2.5
		0	0	0	1	0	1	5
		TO						In 0.5 increments
		1	1	1	1	0	1	31
		1	1	1	1	1	0	31.5
		1	1	1	1	1	1	32

CLK NETWORK



CLK Network Diagram

LM49450 Clock Structure

The MCLK input is first divided by the R divider to product the clock at point B; this is then decoded according to the DAC_MODE to produce a signal which goes to both the DAC digital and the I2S interface, and a signal which goes to the DAC analog.

This table describes the relationship between the clocks, for each of the four possible DAC modes in terms of audio input sampling frequency fs.

TABLE 4. Relationship between clocks for each of the four DAC modes

DAC MODE	Description			
	OSR	CLK at B	DAC Digital CLK	DAC Analog CLK
00	125	250fs	250fs	125fs
01	128	256fs	128fs	128fs
10	64	128fs	128fs	64fs
11	32	128fs	128fs	32fs

Common Clock Settings for the DAC

In DAC_MODE 0, the DAC has an oversampling rate (OSR) of 125 but requires a 250xfs clock at point B. This allows a simple clocking solution as it will work from 12.000MHz (common in most systems with Bluetooth or USB) at 48kHz exactly. In the other DAC modes, the DAC requires a conventional 2^Nxfs clock for conversation. The following table describes the clock required at point B for various clock sample rates in the different DAC modes:

TABLE 5. Common DAC Clock Frequencies

Sample Rate	Clock Required at B (MHz)			
	DAC MODE = 2b00 (OSR = 125fs, Clock Required = 250fs)	DAC MODE = 2b01 (OSR = 128fs, Clock Required = 256fs)	DAC MODE = 2b10 (OSR = 64fs, Clock Required = 128fs)	DAC MODE = 2b11 (OSR = 32fs, Clock Required = 128fs)
8	2	2.084	—	—
11.025	2.75625	2.8224	—	—
12	3	3.072	—	—
16	4	4.096	—	—
22.05	5.5125	5.6448	—	—
24	6	6.144	—	—
32	8	8.192	—	—
44.1	11.025	11.2896	—	—
48	—	12.288	—	—
88.2	—	—	11.2896	—
96	—	—	12.288	—
176.4	—	—	—	22.5792
192	—	—	—	24.576

CHARGE PUMP CLOCK REGISTER (0x02h)

The charge pump clock register sets the charge pump frequency derived from MCLK when the LM49450 is in DAC mode. Default value is for register 02h is 0x49h.

TABLE 6. Charge Pump Clock Register

Bit	Name	Value								Description
B7:B0	CPDIV_7 (B7) CPDIV_6 (B6) CPDIV_5 (B5) CPDIV_4 (B4) CPDIV_3 (B3) CPDIV_2 (B2) CPDIV_1 (B1) CPDIV_0 (B0)	B7	B6	B5	B4	B3	B2	B1	B0	Sets charge pump oscillator frequency in DAC mode (derived from MCLK).
		0	0	0	0	0	0	0	0	Bypass divider
		0	0	0	0	0	0	0	1	1
		0	0	0	0	0	0	1	0	1.5
		0	0	0	0	0	0	1	1	2
		0	0	0	0	0	1	0	0	2.5
		0	0	0	0	0	1	0	1	3
		TO								In 0.5 increments
		1	1	1	1	1	1	0	1	127
		1	1	1	1	1	1	1	0	127.5
		1	1	1	1	1	1	1	1	128

CP_DIV REGISTER

LM49450 Clock Structure

This register is used to control the charge pump clock when the register field LINE_IN_ENABLE is low i.e. DAC mode.

When the register field LINE_IN_ENABLE is high, the Clocks module is held in reset and as a result no CP_CLOCK_C is produced.

TABLE 7. CP_DIV Default Value 0x49h

Bits	Field	Description	
7:0	CP_DIV	Programs the CP divider (devides from an expected 12.000MHz input).	
		CP_DIV	Divide Value
		0	Bypass
		1	1
		2	1.5
		3	2
		4	2.5
		5 to 253	3 to 127
		254	127.5
		255	128

Examples of CP_DIV Values one might use for various sample rates and DAC modes

TABLE 8. Typical CP_DIV Values for DAC Mode 00

MCLK (MHZ)	CP_DIV	Nominal Frequency (Hz)
2	11	333333
2.75625	16	324265
3	17	333333
4	23	333333
5.5125	33	324264
6	36	324324
8	48	326530

MCLK (MHZ)	CP_DIV	Nominal Frequency (Hz)
11.025	67	324265
12	73	324324

TABLE 9. Typical CP_DIV Values for DAC Mode 01

MCLK (MHZ)	CP_DIV	Nominal Frequency (Hz)
2.048	11	341333
2.8224	17	313600
3.072	18	323368
4.096	24	327680
5.6448	33	332047
6.144	37	323368
8.192	49	327680
11.2896	68	327234
12.288	75	323368

TABLE 10. Typical CP_DIV Values for DAC Mode 10

MCLK (MHZ)	CP_DIV	Nominal Frequency (Hz)
11.2896	68	327234
12.288	75	323368

TABLE 11. Typical CP_DIV Values for DAC Mode 11

MCLK (MHZ)	CP_DIV	Nominal Frequency (Hz)
22.5792	138	324881
24.576	150	325510

I2S MODE CONTROL REGISTER (0x03h)

Default value is 0x00h.

TABLE 12. I2S Mode Control Register

Bit	Name	Value			Description
B7	RESERVED	X			Unused
B6:B4	I2S_WRD_2 (B6) I2S_WRD_1 (B5) I2S_WRD_0 (B5)	B6	B5	B4	Sets I^2S word size in Right Justified Mode
		0	0	0	16
		0	0	1	18
		0	1	0	20
		0	1	1	22
		1	0	0	24
		1	0	1	25
		1	1	0	26
		1	1	1	32
B3	I2S_STEREO _REVERSE	0			Normal mode. Left channel data goes to left channel output Right channel data goes to right channel output.
		1			Reverse mode. Left channel data goes to right channel output Right channel data goes to left channel output

Bit	Name	Value		Description
B2	I2S_WORD_ORDER	0		Normal mode. I^{2}S_WS = 0 indicates left channel audio I^{2}S_WS = 1 indicates right channel audio
		1		Reverse mode. I^{2}S_WS = 0 indicates right channel audio I^{2}S_WS = 1 indicates left channel audio.
B1:B0	I2S_MODE_1 (B1) I2S_MODE_0 (B0)	B1	B0	Sets I^{2}S operating mode
		0	0	Normal Mode
		0	1	Left Justified Mode
		1	0	Right Justified Mode
		1	1	Unused

I2S CLOCK REGISTER (0x04h)

Default value is 0x00h.

TABLE 13. I2S Clock Register

Bit	Name	Value				Description	
B7:B4	I2S_CLK_3 (B7) I2S_CLK_2 (B6) I2S_CLK_1 (B5) I2S_CLK_0 (B4)	B7	B6	B5	B4	Sets divider ratio to derive the I^{2}S clock from the divided MCLK in I^{2}S master mode	
						DIVIDE BY	RATIO
		0	0	0	0	1	—
		0	0	0	1	2	—
		0	0	1	0	4	—
		0	1	1	1	6	—
		0	0	0	0	8	—
		0	0	1	1	10	—
		0	1	0	0	16	—
		0	1	1	1	20	—
		1	0	0	0	2.5	2.5
		1	0	0	1	3	1:3
		1	0	1	0	3.90625	32:125
		1	0	1	1	5	1:5
		1	1	0	0	7.8125	16:125
		1	1	0	1	—	—
		1	1	1	0	—	—
		1	1	1	1	—	—
B3:B2	I2S_WS_1 (B3) I2S_WS_0 (B2)	B3		B2		Determines the bit length per data word of I^{2}S_WS in I^{2}S master mode	
		0		0		16	
		0		1		25	
		1		0		32	
		1		1		—	
B1	I2S_WS_MS	0				I^{2}S WS slave mode. The LM49450 drives the I^{2}S WS signal from the I2S_WS line.	
		1				I^{2}S WS master mode. The LM49450 generates the I2S WS signal. I2S_WS line is driven by the LM49450	
B0	I2S_CLK_MS	0				I^{2}S clock slave mode. The LM49450 derives its I^{2}S clock from the I2S_CLK line.	
		1				I^{2}S clock master mode. The LM49450 generates the I^{2}S clock signal. I2S_CLK line is driven by the LM49450.	

HEADPHONE 3D CONFIGURATION REGISTER (0x05h)

Default value is 0x00h.

TABLE 14. Headphone 3D Configuration Register

Bit	Name	Value		Description
B7	RESERVED	X		UNUSED
B6	HP_3DATTN	0		No Attenuation
		1		Output signals are attenuated by 6dB
B5:B4	HP_3DFREQ_1 (B5) HP_3DFREQ_0 (B4)	B5	B4	Sets 3D high pass filter -3dB (roll-off) frequency
		0	0	0
		0	1	300Hz
		1	0	600Hz
		1	1	900Hz
B3:B2	HP_3DFREQ_1 (B3) HP_3DFREQ_0 (B2)	B3	B2	Sets the 3D mix level, ie the amount of the left channel signal that appears on the right channel and visa versa.
		0	0	25%
		0	1	37.5%
		1	0	50%
		1	1	75%
B1	HP_3D	0		Narrow 3D effect
		1		Wide 3D effect
B0	HP_3DEN	0		Headphone 3D disabled
		1		Headphone 3D enabled

LOUDSPEAKER 3D CONFIGURATION REGISTER (0x06h)

Default value is 0x00h.

TABLE 15. Loudspeaker 3D Configuration Register

Bit	Name	Value		Description
B7	RESERVED	X		UNUSED
B6	LS_3DATTN	0		No Attenuation
		1		Output signals are attenuated by 6dB
B5:B4	LS_3DFREQ_1 (B5) LS_3DFREQ_0 (B4)	B5	B4	Sets 3D high pass filter -3dB (roll-off) frequency
		0	0	0
		0	1	300Hz
		1	0	600Hz
		1	1	900Hz
B3:B2	LS_3DFREQ_1 (B3) LS_3DFREQ_0 (B2)	B3	B2	Sets the 3D mix level, ie the amount of the left channel signal that appears on the right channel and visa versa.
		0	0	25%
		0	1	37.5%
		1	0	50%
		1	0	75%
B1	HP_3D	0		Narrow 3D effect
		1		Wide 3D effect
B0	HP_3DEN	0		Loudspeaker 3D disabled
		1		Loudspeaker 3D enabled

HEADPHONE VOLUME CONTROL REGISTER (0x07h)

Default value is 0x00h.

TABLE 16. Headphone Volume Control Register

Bit	Name	Value	Description
B7:B5	RESERVED	X	UNUSED
B4:B0	HP4 (B4) HP3 (B3) HP2 (B2) HP1 (B1) HP0 (B0)	See Headphone Volume Control Table	Controls gain/attenuation of the audio signal in the headphone path.

VOLUME STEP	HP4	HP3	HP2	HP1	HP0	HP GAIN (dB)
1	0	0	0	0	0	–59
2	0	0	0	0	1	–48
3	0	0	0	1	0	–40.5
4	0	0	0	1	1	–34.5
5	0	0	1	0	0	–30
6	0	0	1	0	1	–27
7	0	0	1	1	0	–24
8	0	0	1	1	1	–21
9	0	1	0	0	0	–18
10	0	1	0	0	1	–15
11	0	1	0	1	0	–13.5
12	0	1	0	1	1	–12
13	0	1	1	0	0	–10.5
14	0	1	1	0	1	–9
15	0	1	1	1	0	–7.5
16	0	1	1	1	1	–6
17	1	0	0	0	0	–4.5
18	1	0	0	0	1	–3
19	1	0	0	1	0	–1.5
20	1	0	0	1	1	0
21	1	0	1	0	0	1.5
22	1	0	1	0	1	3
23	1	0	1	1	0	4.5
24	1	0	1	1	1	6
25	1	1	0	0	0	7.5
26	1	1	0	0	1	9
27	1	1	0	1	0	10.5
28	1	1	0	1	1	12
29	1	1	1	0	0	13.5
30	1	1	1	0	1	15
31	1	1	1	1	0	16.5
32	1	1	1	1	1	18

LOUDSPEAKER VOLUME CONTROL REGISTER (0x08h)

Default value is 0x00h.

TABLE 17. Loudspeaker Volume Control Register

Bit	Name	Value	Description
B7:B5	RESERVED	X	UNUSED
B4:B0	LS4 (B4) LS3 (B3) LS2 (B2) LS1 (B1) LS0 (B0)	See Loudspeaker Volume Control Table	Controls gain/attenuation of the audio signal in the loudspeaker path.

VOLUME STEP	LS4	LS3	LS2	LS1	LS0	LS GAIN (dB)
1	0	0	0	0	0	–53
2	0	0	0	0	1	–42
3	0	0	0	1	0	–34.5
4	0	0	0	1	1	–28.5
5	0	0	1	0	0	–24
6	0	0	1	0	1	–21
7	0	0	1	1	0	–18
8	0	0	1	1	1	–15
9	0	1	0	0	0	–12
10	0	1	0	0	1	–9
11	0	1	0	1	0	–7.5
12	0	1	0	1	1	–6
13	0	1	1	0	0	–4.5
14	0	1	1	0	1	–3
15	0	1	1	1	0	–1.5
16	0	1	1	1	1	0
17	1	0	0	0	0	1.5
18	1	0	0	0	1	3
19	1	0	0	1	0	4.5
20	1	0	0	1	1	6
21	1	0	1	0	0	7.5
22	1	0	1	0	1	9
23	1	0	1	1	0	10.5
24	1	0	1	1	1	12
25	1	1	0	0	0	13.5
26	1	1	0	0	1	15
27	1	1	0	1	0	16.5
28	1	1	0	1	1	18
29	1	1	1	0	0	19.5
30	1	1	1	0	1	21
31	1	1	1	1	0	22.5
32	1	1	1	1	1	24

DAC COMPENSATION FILTER REGISTERS (0x09h to 0x0Eh)

DAC Compensation Filter

The LM49450 DAC features a 5 band FIR filter that can be used as an equalizer for the digital audio path. Registers 0x09h, 0x0Ah, 0x0Bh, 0x0Ch, 0x0Dh, and 0x0Eh provide an 8-bit control for each individual FIR filter.

EXTERNAL COMPONENT SELECTION

The LM49450 uses different supplies for each portion of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The speaker amplifier gain stage is powered from V_{DD}, while the output stage is powered from LSV_{DD}. The headphone amplifiers, input amplifiers and volume control stages are powered from HPV_{DD}. The separate power supplies allow the speakers to operate from a higher voltage for maximum headroom, while the headphones operate from a lower voltage, improving power dissipation. HPV_{DD} may be driven by a linear regulator to further improve performance in noisy environments. The I^2C portion if powered from I^2CV_{DD}, allowing the I^2C portion of the LM49450 to interface with lower voltage digital controllers.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing and Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Typical applications employ a voltage regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM49450 supply pins. A 1µF ceramic capacitor placed close to each supply pin is recommended.

Bypass Capacitor Selection

The LM49450 internally generates a $V_{DD}/2$ common-mode bias voltage. The BYPASS capacitor CBYPASS, improves PSRR and THD+N by reducing noise at the BYPASS node. Use a 2.2µF ceramic placed as close to the device as possible.

REF Capacitor Selection

The LM49450 generates an internal low noise reference voltage used by the DAC. For best THD+N performance, bypass REF with 10µF and 0.1µF ceramic capacitors.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems where low maximum output power requirements.

Charge Pump Hold Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV_{SS}. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems where low maximum output power requirements.

Input Capacitor Selection

The LM49450 analog inputs require input coupling capacitors. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49450. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation (1) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (1)$$

Where the value of R_{IN} is typically 20kΩ.

The input capacitors can also be used to remove low frequency content from the audio signal. Small speakers cannot reproduce, and may even be damaged by low frequencies. High pass filtering the audio signal helps protect the speakers. When the LM49450 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

PCB Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM49450 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

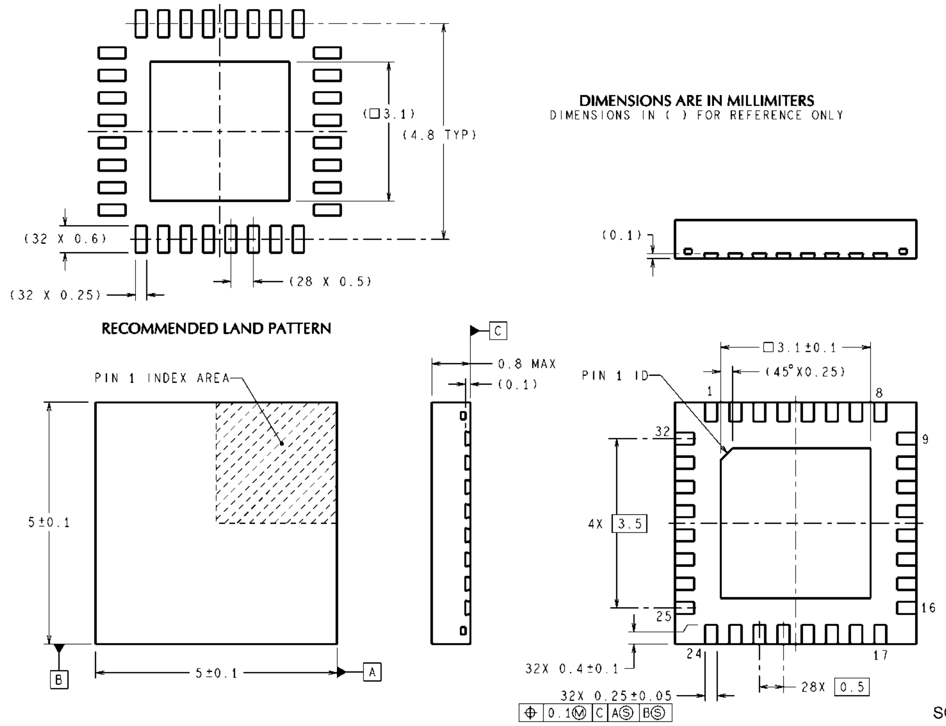
Exposed DAP Mounting Considerations

The LM49450 LLP package features an exposed die-attach (thermal) pad on its backside. The exposed pad provides a direct heat conduction path from the die to the PCB, reducing the thermal resistance of the package. Connect the exposed pad to GND with a large pad and via to a large GND plane on the bottom of the PCB for best heat distribution.

Revision Table

Rev	Date	Description
1.0	12/18/07	Initial release.
1.01	09/26/08	Corrected the package drawing.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA32A (Rev A)

32 Lead LLP
Order Number LM49450SQ
NS Package Number SQA32A

Notes

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